



IBM Field Engineering

Maintenance Diagrams

2020 Processing Unit

System/360 Model 20

(Machines with serial no. 50,000 and above)

Volume 2

Preface

This publication (Volume 2) and its companion publication (Volume 1, Form Y33-1024) constitute the Field Engineering Maintenance Diagrams manual for the IBM 2020 Processing Unit (machines with serial number 50,000 and above) in the IBM System/360 Model 20. Volume 2 contains operations information (Section 5) and Volume 1 contains information on the following:

- Diagnostic techniques (Section 1)
- Error conditions (Section 2)
- Data flow (Section 3)
- Functional units (Section 4)
- Power (Section 6)
- Microprograms (Appendix B)

Both volumes are used for maintenance, instruction, and recall.

The material in these volumes supplements the information contained in the following manuals:

1. Field Engineering Theory of Operation, *2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1021.
2. Field Engineering Maintenance Manual, *2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1035.

Associated Publications

The following Field Engineering Maintenance Diagrams manuals contain information on the features which may be installed on the 2020 Processing Unit:

1. *1403 Printer Models 2, 7, N1 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1018.
2. *2152 Printer-Keyboard Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1026.
3. *2203 Printer Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1022.
4. *2520 Card Read Punch Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1028.

5. *2560 Multi-Function Card Machine Attachment Feature, 2501 Card Reader Attachment Feature, 1442 Card Punch Model 5 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1033.

6. *Binary Synchronous Communications Adapter, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1039.

7. *Input/Output Channel Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1017.

8. *Storage Control Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1037.

Information on the serial I/O channel feature is contained in Field Engineering Theory of Operation, Maintenance Diagrams, *Serial I/O Channel Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1040.

The associated Field Engineering Theory of Operations manual for the features are:

1. *1403 Printer Models 2, 7, N1 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1020.

2. *2152 Printer-Keyboard Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1025.

3. *2203 Printer Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1027.

4. *2520 Card Read Punch Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1029.

5. *2560 Multi-Function Card Machine Attachment Feature, 2501 Card Reader Attachment Feature, 1442 Card Punch Model 5 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1034.

6. *Binary Synchronous Communications Adapter, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1038.

7. *Input/Output Channel Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1019.

8. *Storage Control Feature, System/360 Model 20 (Machines with serial no. 50,000 and above)*, Form Y33-1036.

Second Edition (November 1969)

This volume is a major revision of, and obsoletes, Y33-1042-0.

Changed diagrams are denoted by the symbol ● to the left of the caption, small changes being also indicated by vertical lines to the left of the changes.

Changes are continually made to the specifications herein; any such changes will be reported in subsequent revisions or FE Supplements.

A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Laboratories, Product Publications, Dept 784, 703 Boeblingen/Wuertt, P.O. Box 210, Germany.

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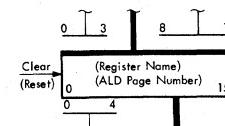
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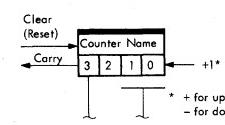
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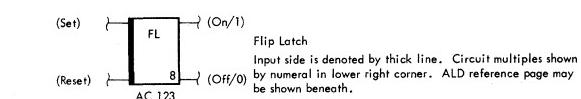
Note: The diagrams in this manual have a code number to the right of the caption.
This is a publishing control number and is unrelated to the subject matter.

Legend**1. Logic Diagrams**

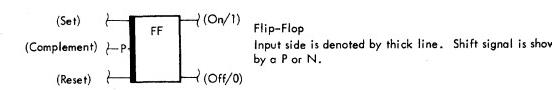
Register, Counter
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.



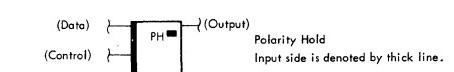
Counter
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.



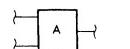
Flip Latch
Input side is denoted by thick line. Circuit multiples shown by numeral in lower right corner. ALD reference page may be shown beneath.



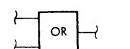
Flip-Flop
Input side is denoted by thick line. Shift signal is shown by a P or N.



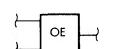
Polarity Hold
Input side is denoted by thick line.



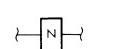
AND



OR



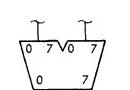
Exclusive OR



Negator (Inverter)



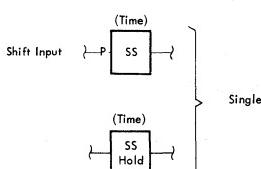
Negative Polarity wedge



Adder



Gate
Numerals against gate symbol give page or diagram number of gating circuit.



Shift Input

SS

Hold

Single shot



Oscillator



Time Delay



Indicator lamp



Indicatable flip latch



Parity Check data bus



Parity Generate data bus



Amplifier

XX Abbreviations:

CD = Core Driver

HD = Head Driver

ID = Indicator Driver

LD = Line Driver

LT = Line Terminator

MD = Magnet Driver

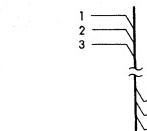
V = Voltage Amplifier



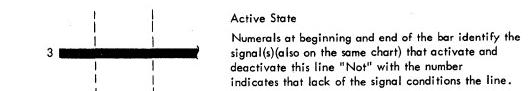
Interface

I/O IP

Denotes interface between two units.



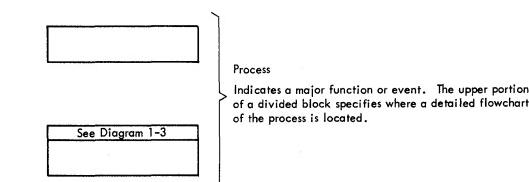
Multiple Line Transfer

2. Timing Charts

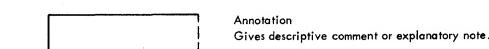
Active State
Numerals at beginning and end of the bar identify the signal(s)(also on the state chart) that activate and deactivate this line "Not" with the number indicates that lack of the signal conditions the line.

3. Flowcharts

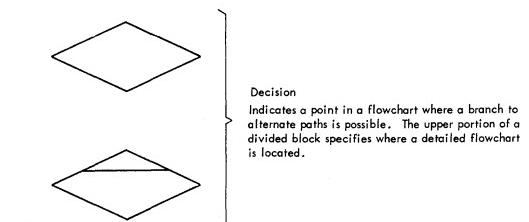
Terminal
Indicates beginning or end of event



Process
Indicates a major function or event. The upper portion of a divided block specifies where a detailed flowchart of the process is located.

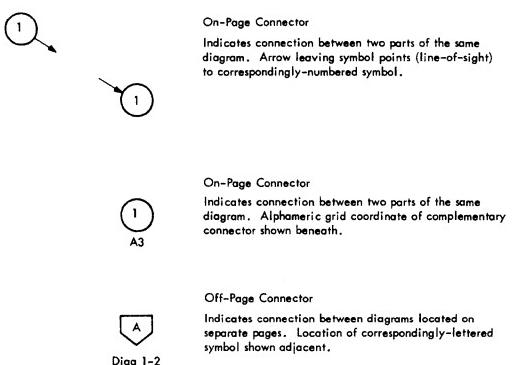


Annotation
Gives descriptive comment or explanatory note.

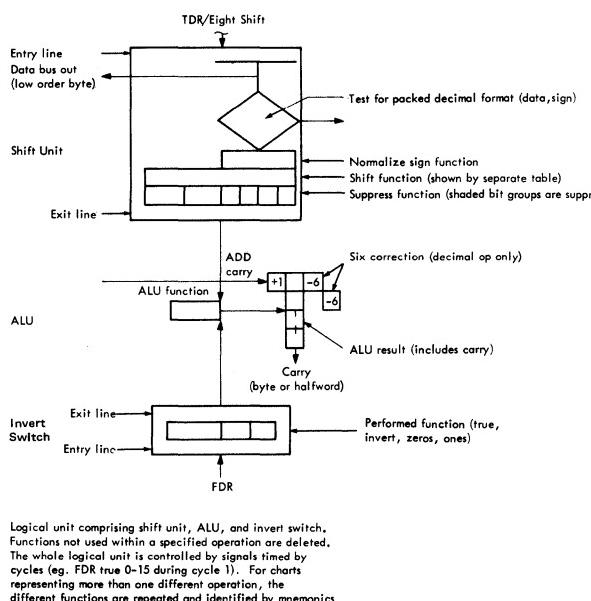
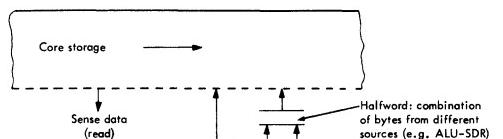
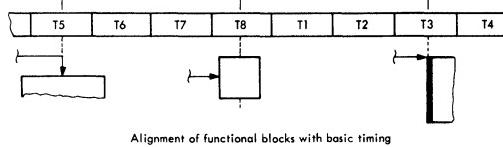
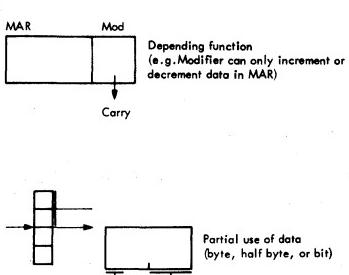
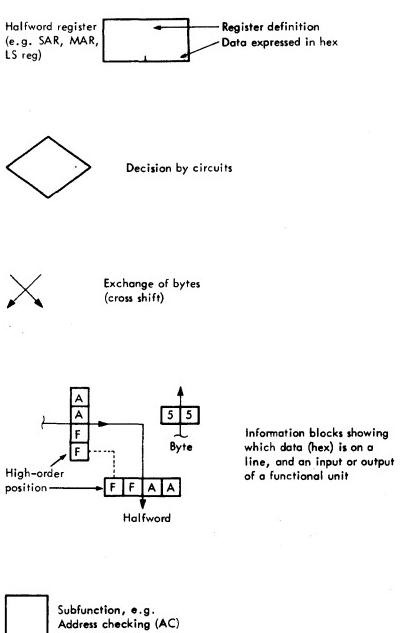


Decision
Indicates a point in a flowchart where a branch to alternate paths is possible. The upper portion of a divided block specifies where a detailed flowchart of the decision is located.

4. General



5. Special Symbols

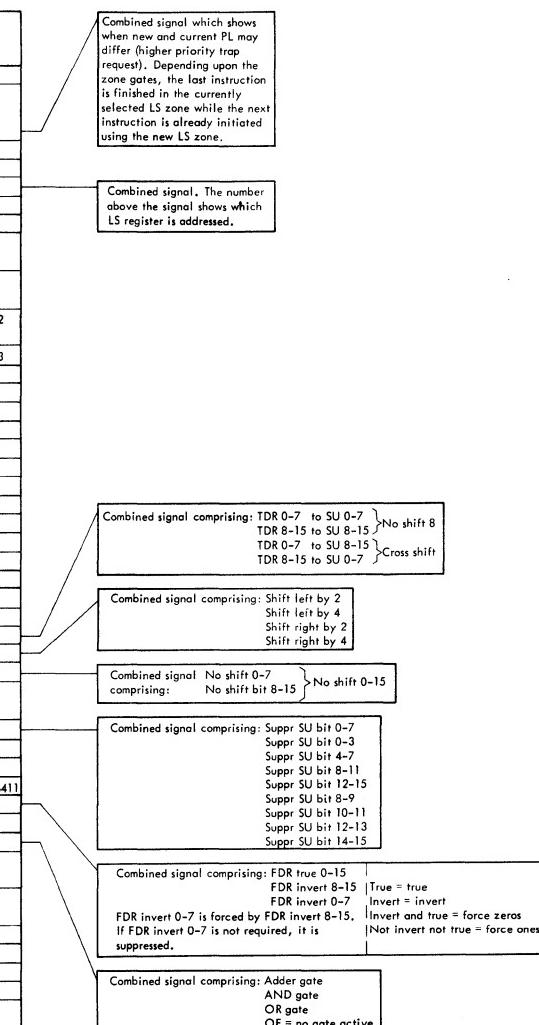


6. Standard Signal Arrangement

Signal grouping according to functional units		ALD
LS zone selection	1 Sense Trap Request Lines	LA103
	2 LS New PL Zone Gate	KA511
	3 LS Current PL Zone Gate	
	4 New/Current PL	
	5 CE LS Select	CC222
Spore	6	
	7 Fixed X-Address	LA412
	8 'To Reg' Select	LA402
	9 'From Reg' Select	LA411
	10 LS to SAR	KB411
	11 LS to MAR	KB401
	12 LS to FDR	
	13 LS to TDR	
	14 MAR to LS	LA702-712
	15 Set ALU I/O Bus to LS	
	16 LS Write	LA302/313
	17	
	18 Set Address Check	RA501
	19 Branch Go	RA502
	20 Increment by 1	RA402
Mar/modifier control	21 Increment by 2	RA403
	22 Decrement by 1	RA401
	23 Decrement by 2	RA402
	24 Prevent Mod-SAR-Inh Check	KA511
SDR control	25	
	26 Prevent Storage Use	MA402
	27 SDR to Inh	MA401
	28 SDR to Op Reg	KB102
TDR/shift unit control	29	
	30 SDR to TDR	KB402
	31 Eight Shift Control	RB162
	32 Shift by 2 or 4	RB161
	33 No Shift	RB162
	34 Test Packed Byte or Sign	RA502
	35 Normalize Sign Active	
ALU control	36 Suppress	RB171
	37	
	38 ALU to FDR	AA303
	39 Reset FDR/Retain FDR 0-7	AA303/KB411
	40 Invert Switch Control	RB301
	41	
	42 ALU Control Gate	AA301
I/O bus control	43 Additional Carry	AA302
	44 Six Correction 8-11/12-15	
	45 Set Carry Latch	AA402
	46 Set Condition Code Latches	
	47 ALU to Inh	MA401
	48 ALU to SAR	KB411
	49	
	50 Data Switch to Op Reg	KB402
	51 Op Reg to Address Bus	KA541
	52 I/O Display Address Out	
	53 Allow Strobe	
	54 SENS Strobe/Control Strobe	BA102
	55 Sense Reset/CTRL Strobe	
Set CPU checks	56 Prevent ALU and SU Check	BA103
	57 I/O Bus to FDR	
	58	
	59	
	60	
	61	
	62	
	63	
	64	
	65	
Set CPU checks	66	
	67 Set ALU Test Latch	CC121
	68 Set Process Check	CC122
	69 Set LSA Check	CC221
	70 Set Mod Check	CC101
	71 Set SU Check	CC102
	72 Set ALU Check	
	73 Set Bus Check	
	74 Set SAR Check	CC101
	75 Set Inh Check	

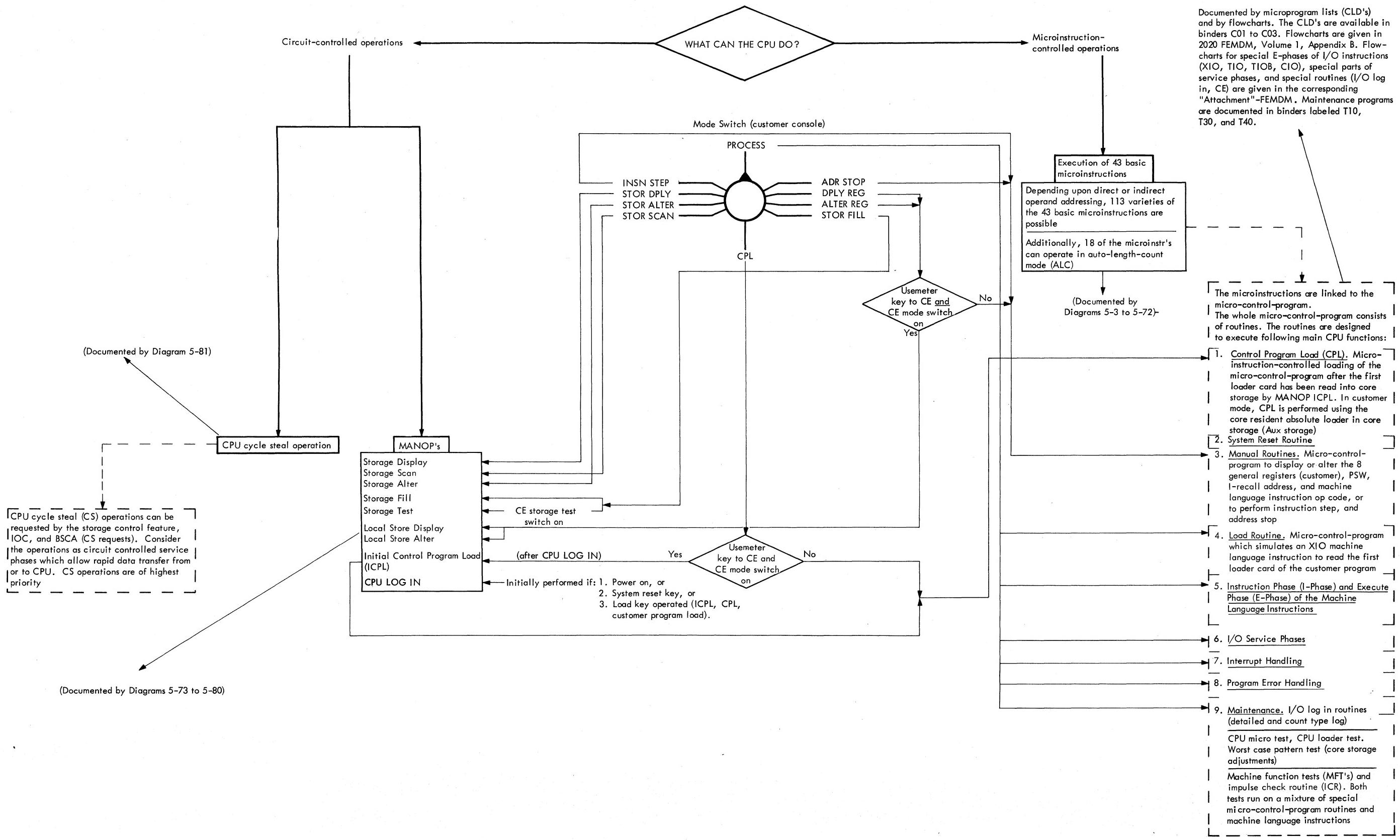
Signals prefixed by "Set" are internal card signals which cannot be measured. They indicate when the specified function is executed.

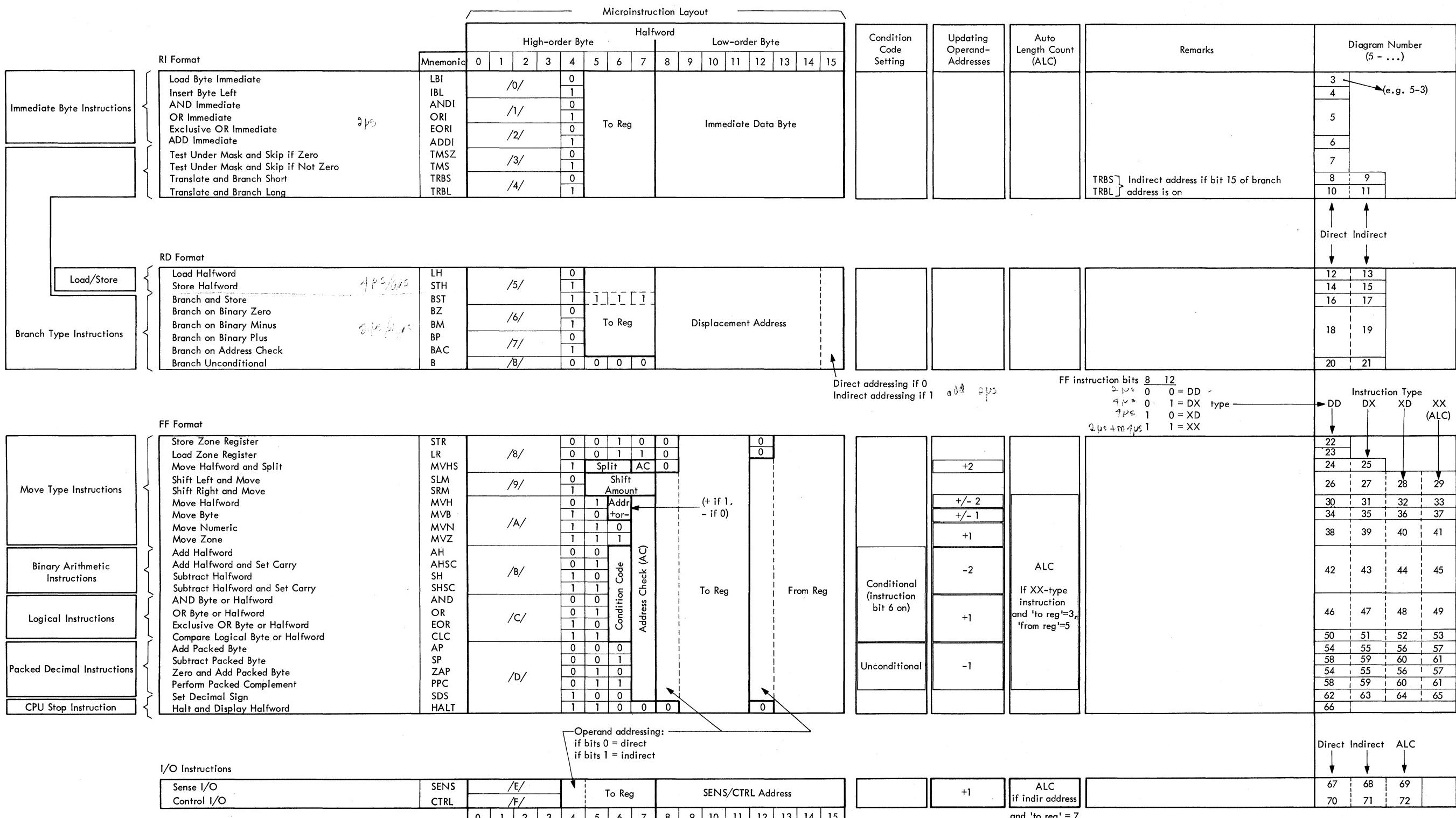
Reference to a single ALD page or to the first of a group of pages.



Abbreviations

AC	Address Check	MANOP	(Circuit-Controlled) Manual Operation
ADDR, Addr, ADR	Address	MAR	Modify Address-Register
ALC	Auto Length Count	MFT	Machine Function Test
ALU	Arithmetic and Logic Unit	Mnem	Mnemonic
ASCII	American Standard Code for Information Interchange		
Aux	Auxiliary	NSI	Next Sequential Instruction
BSCA	Binary Synchronous Communications Adapter	OE	Exclusive OR
CC	Condition Code	Op	Operation
CE	Customer Engineer	Op Reg	Operation Register
Chk, Ck	Check	Oprnd	Operand
CLD	Control Logic Diagram (microprogram list)	PL	Program Level
Col Bin	Column Binary	Pri	Primary
CPL	Control Program Load	PSW	Program Status Word
CPU	Central Processing Unit	Rd	Read
CS	Cycle Steal	Reg	Register
Cust	Customer	Req	Request
CY	Cycle	Rst	Reset
Diag	Diagnostic, Diagram	SAR	Storage Address Register
Displ, Dply	Display	SC	Set Carry
DR	Data Register (display customer console)	SDR	Storage Data Register
EBCDIC	Extended Binary-Coded-Decimal Interchange Code	Stor	Storage
Ex	Execution	SU	Shift Unit
FDR	From-Data Register	Sw	Switch
FL	Flip Latch (Latch)	Syst	System
IAR	(Micro) Instruction Address Register	T	Time (pulse)
ICPL	Initial Control Program Load	TDR	To-Data Register
ICR	Impulse Check Routine	u-instr	Microinstruction
Indir	Indirect	Wkg	Working
Inh	Inhibit (switch)	△ CY	Delta Cycle
Insn, Instr	Instruction	/.../	Representation of Hexadecimal Numbers
IOC	Input/Output Channel		
I/O	Input/Output (Device)		
I-Recall Addr	Instruction-Recall Address		
LC	Length Count		
LS	Local Store		





ADDRESS CHECK (AC, bit 7 of FF format instructions).

When the bit is on, the operand addresses (in 'to' or 'from reg' if indirect address) are checked that they are not outside customer storage area. For halfword instructions (e.g. MVHS, MVH, AH), the addresses are also checked for halfword boundary (address must be even). An address check stops the CPU by program check (trap request 2).

SPLIT (bits 5 and 6 of MVHS).

During MVHS, a halfword is split. The result of the split is set into two adjacent registers. The binary value of bits 5 and 6 (0-3) defines the split mode. Details of split are given in the MVHS flowchart.

SHIFT AMOUNT (bits 5, 6, and 7 of SLM, SRM).

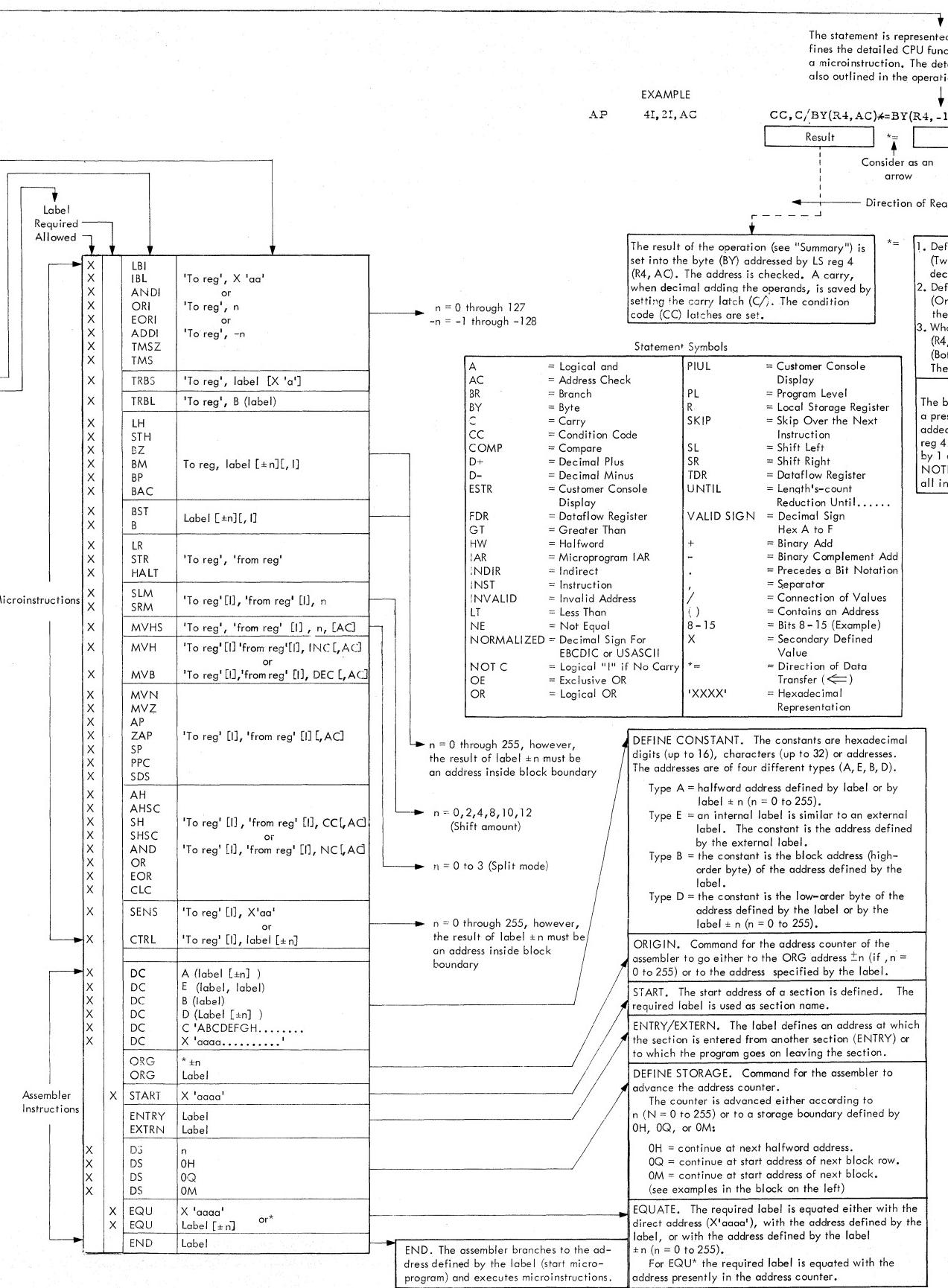
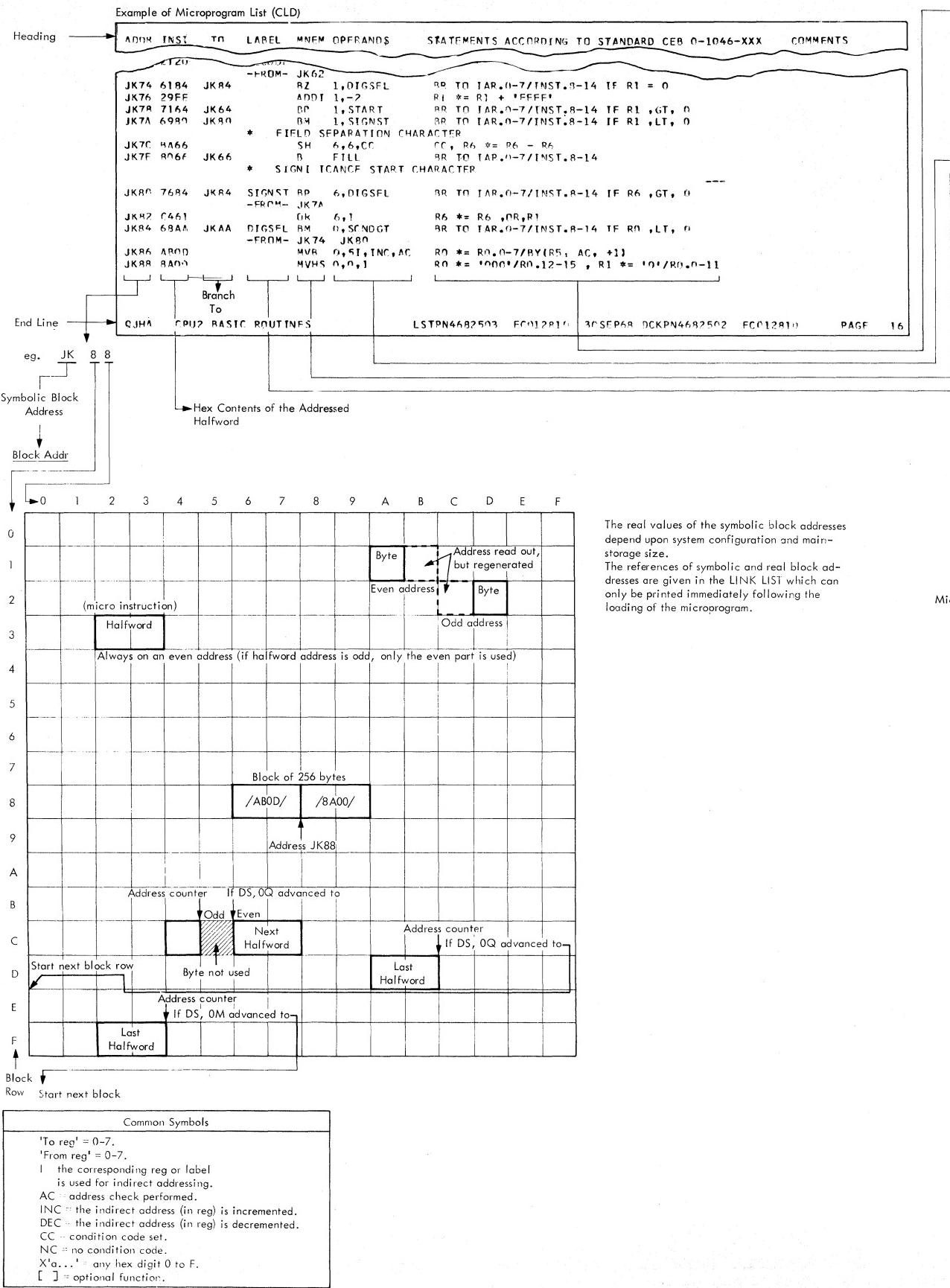
The pattern in these bits specifies the number of bits by which the operand halfword has to be shifted.

Bits 5 6 7	0 0 0	Shift by 0 (No shift, only move)
0 0 1	Shift by 2	
0 1 0	Shift by 4	No shift by 6 (bits 6 and 7 on simultaneously)
1 0 0	Shift by 8	
1 0 1	Shift by 10	
1 1 0	Shift by 12	

'TO REG', 'FROM REG'.

These fields may contain any binary value from 0 to 7. This binary value is used to select one of eight local storage registers in a local store zone. For FF and I/O instructions, the selected register is used as data register if the high-order bit in the 'to or from reg' field is off (direct addressing). The selected register is used as address register for a core storage operand if the high-order bit is on (indirect addressing).

When the 'to reg' specifies local store register 7 (IAR, instruction address register), instructions which set data into a local store register as a result of their operation (load type instruction) are treated as no operation.



Instructions	
Mnemonic	Diagram
ADDI	5-6
AH	5-42, 43, 44, 45
AHSC	5-42, 43, 44, 45
AND	5-46, 47, 48, 49
ANDI	5-5
AP	5-54, 55, 56, 57
B	5-20, 21
BAC	5-18, 19
BM	5-18, 19
BP	5-18, 19
BST	5-16, 17
BZ	5-18, 19
CLC	5-50, 51, 52, 53
CTRL	5-70, 71, 72
EOR	5-46, 47, 48, 49
EORI	5-5
HALT	5-66
IBL	5-4
LBI	5-3
LH	5-12, 13
LR	5-23
MVB	5-34, 35, 36, 37
MVH	5-30, 31, 32, 33
MVHS	5-24, 25
MVN	5-38, 39, 40, 41
MVZ	5-38, 39, 40, 41
OR	5-46, 47, 48, 49
ORI	5-5
PPC	5-58, 59, 60, 61
SDS	5-62, 63, 64, 65
SENS	5-67, 68, 69
SH	5-42, 43, 44, 45
SHSC	5-42, 43, 44, 45
SLM	5-26, 27, 28, 29
SP	5-58, 59, 60, 61
SRM	5-26, 27, 28, 29
STH	5-14, 15
STR	5-22
TMS	5-7
TMSZ	5-7
TRBL	5-10, 11
TRBS	5-8, 9
ZAP	5-54, 55, 56, 57

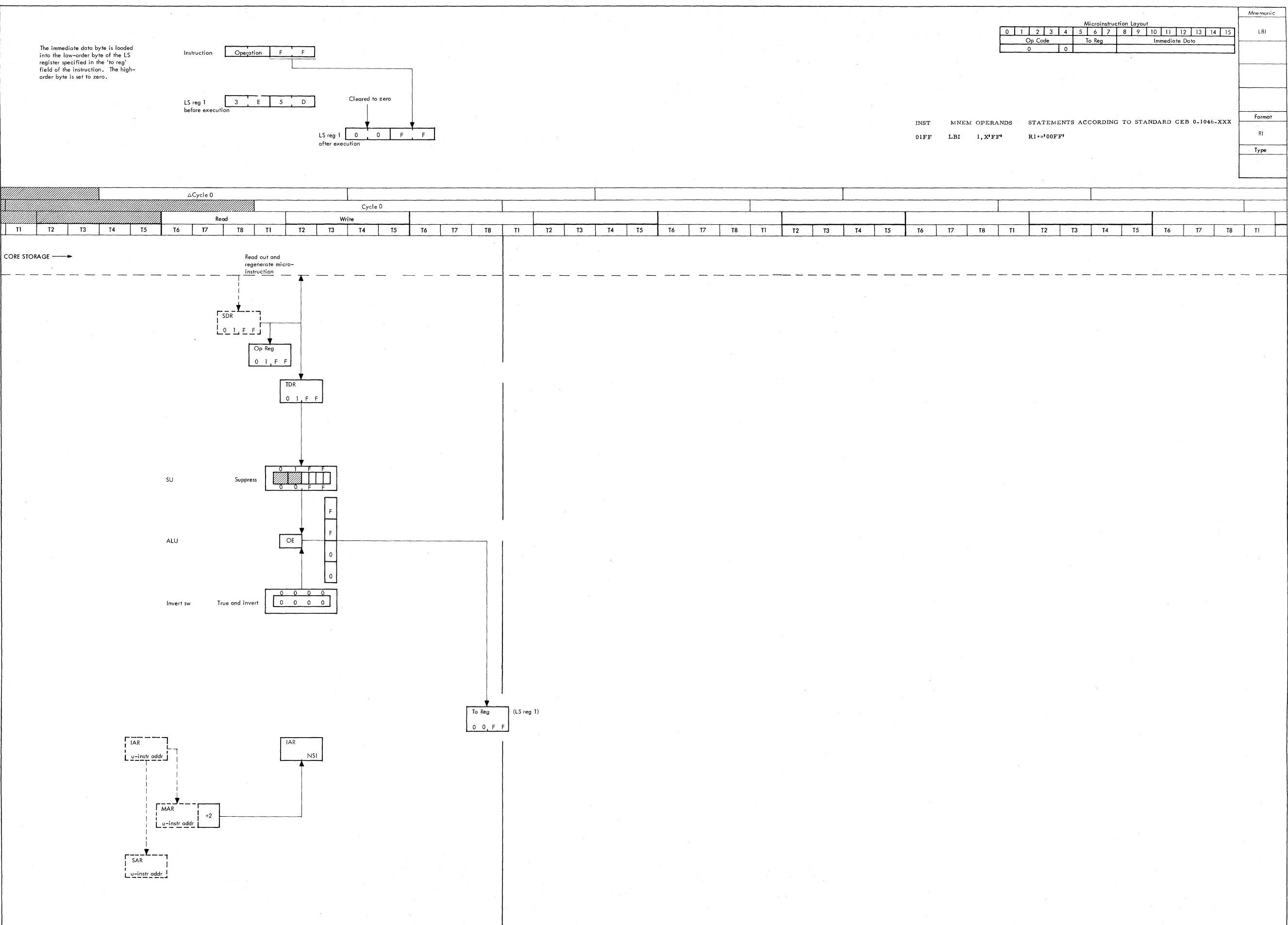
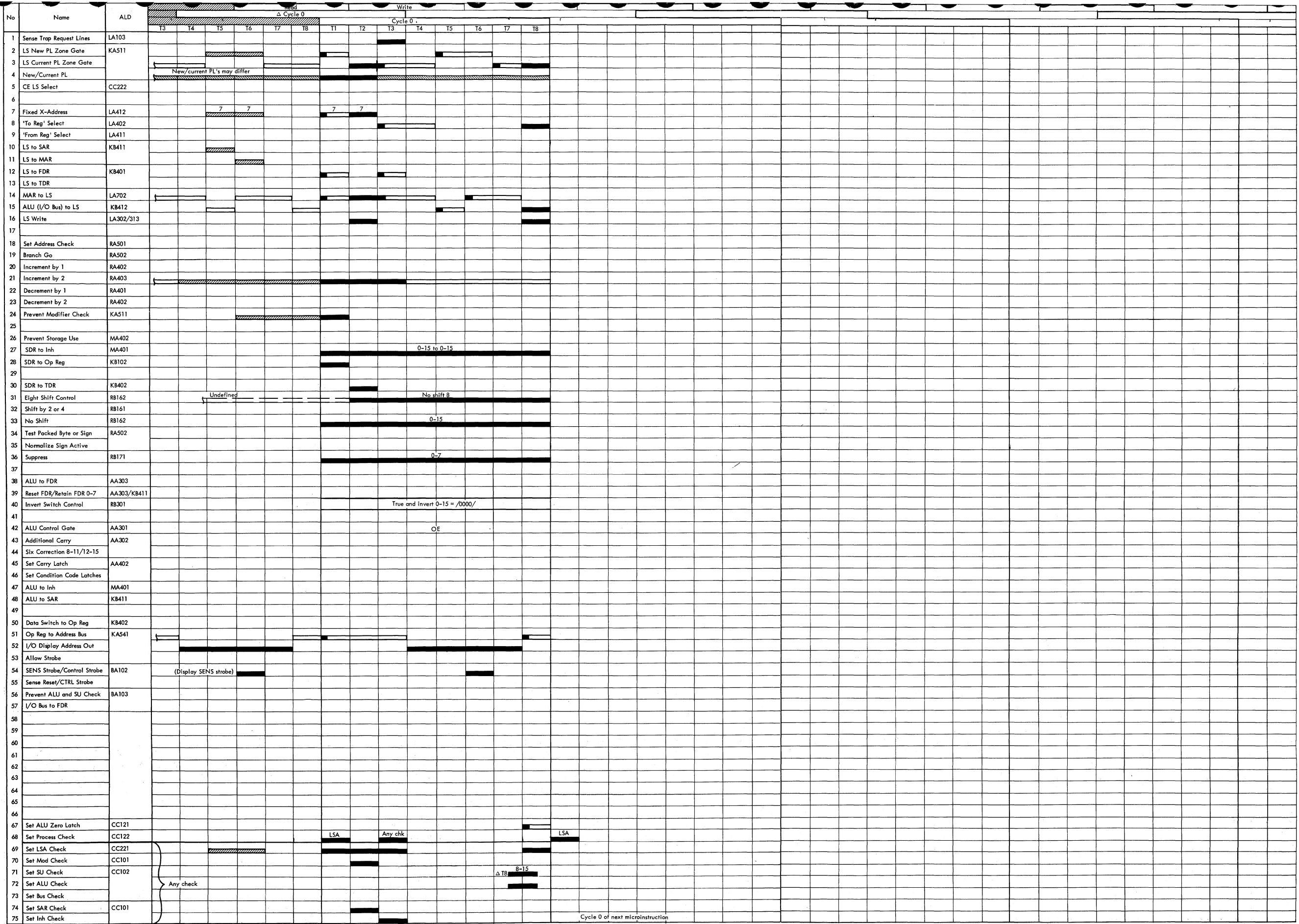
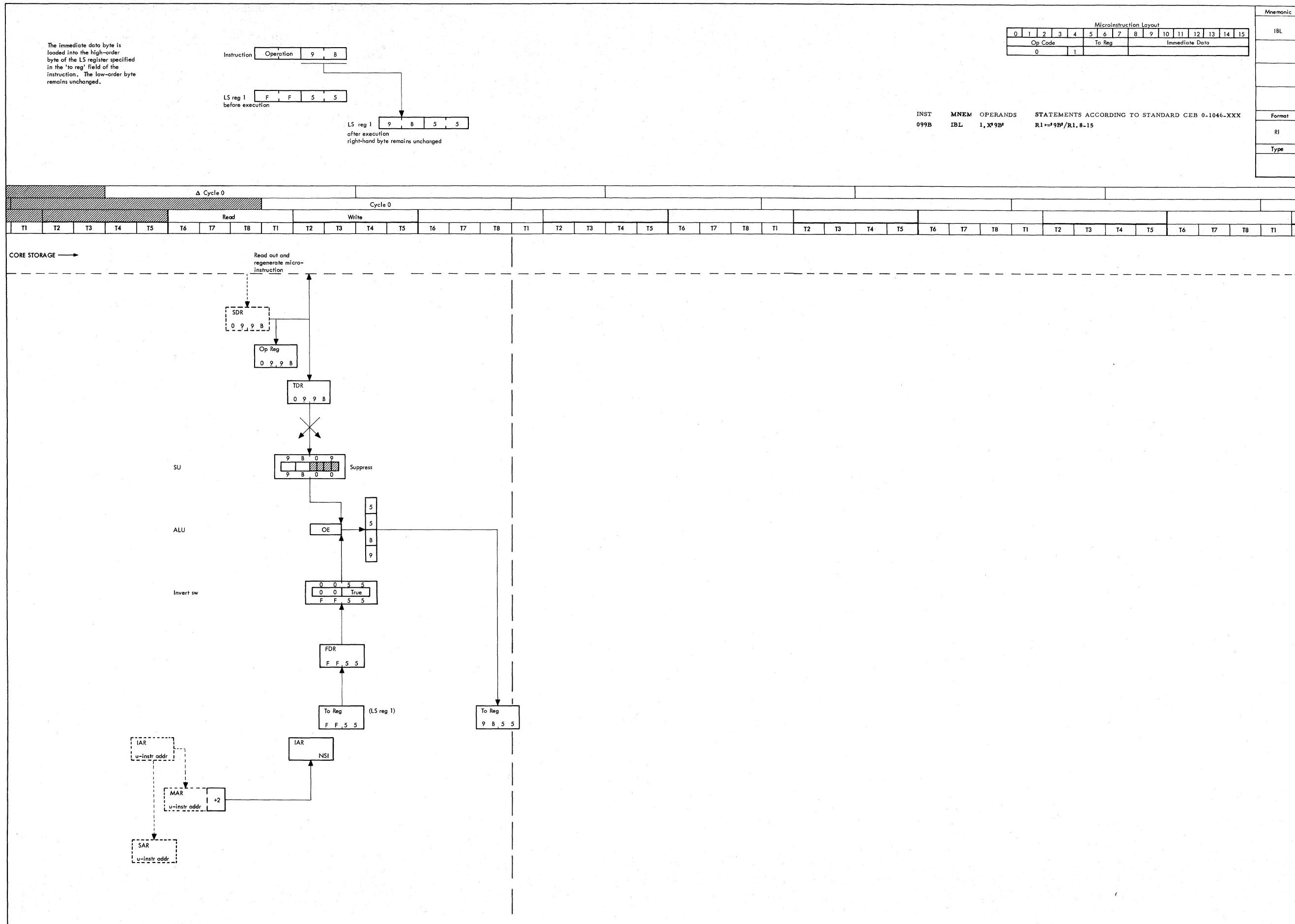


Diagram 5-3. Load Byte Intermediate (Part 1 of 2) (03708) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

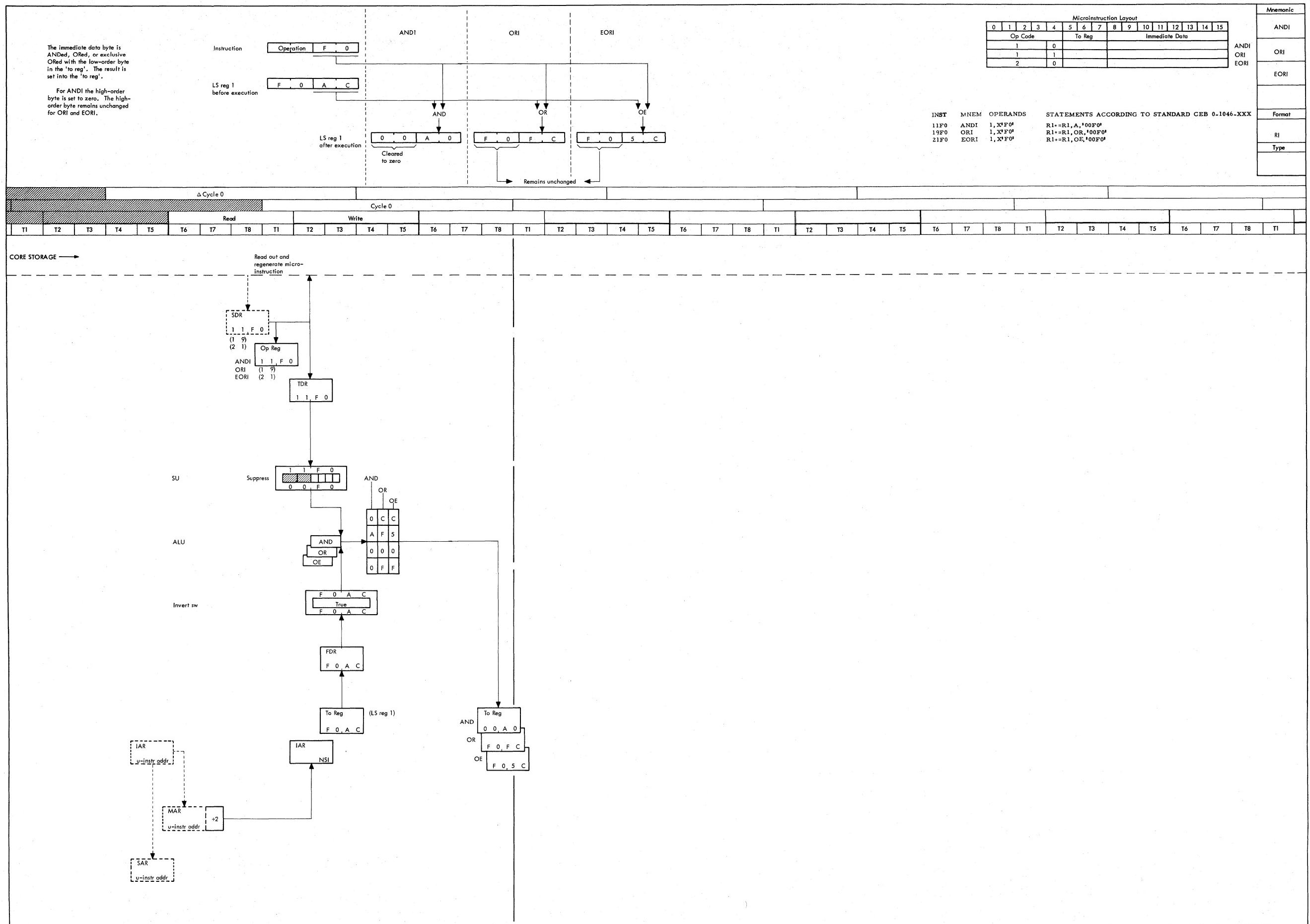




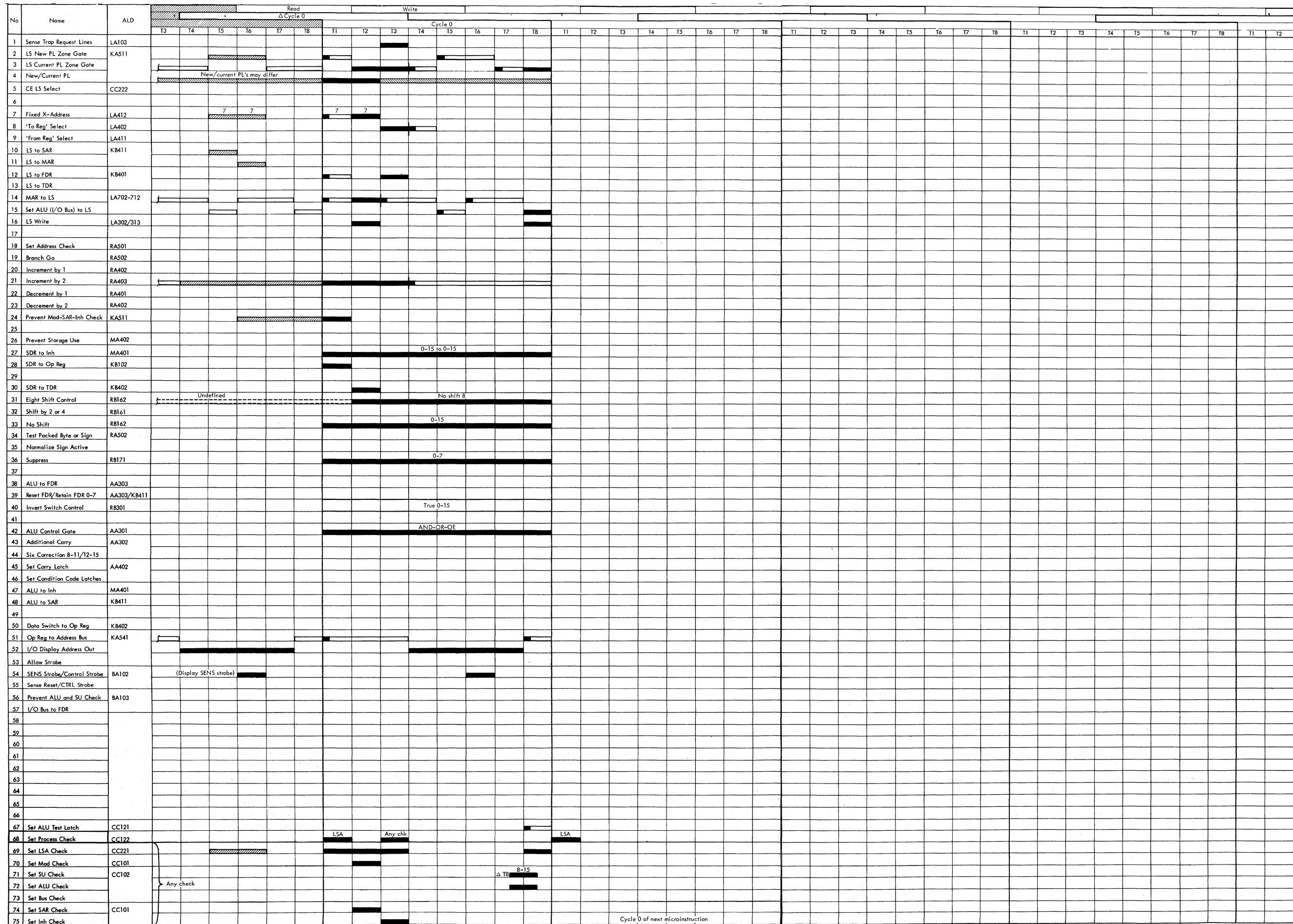
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

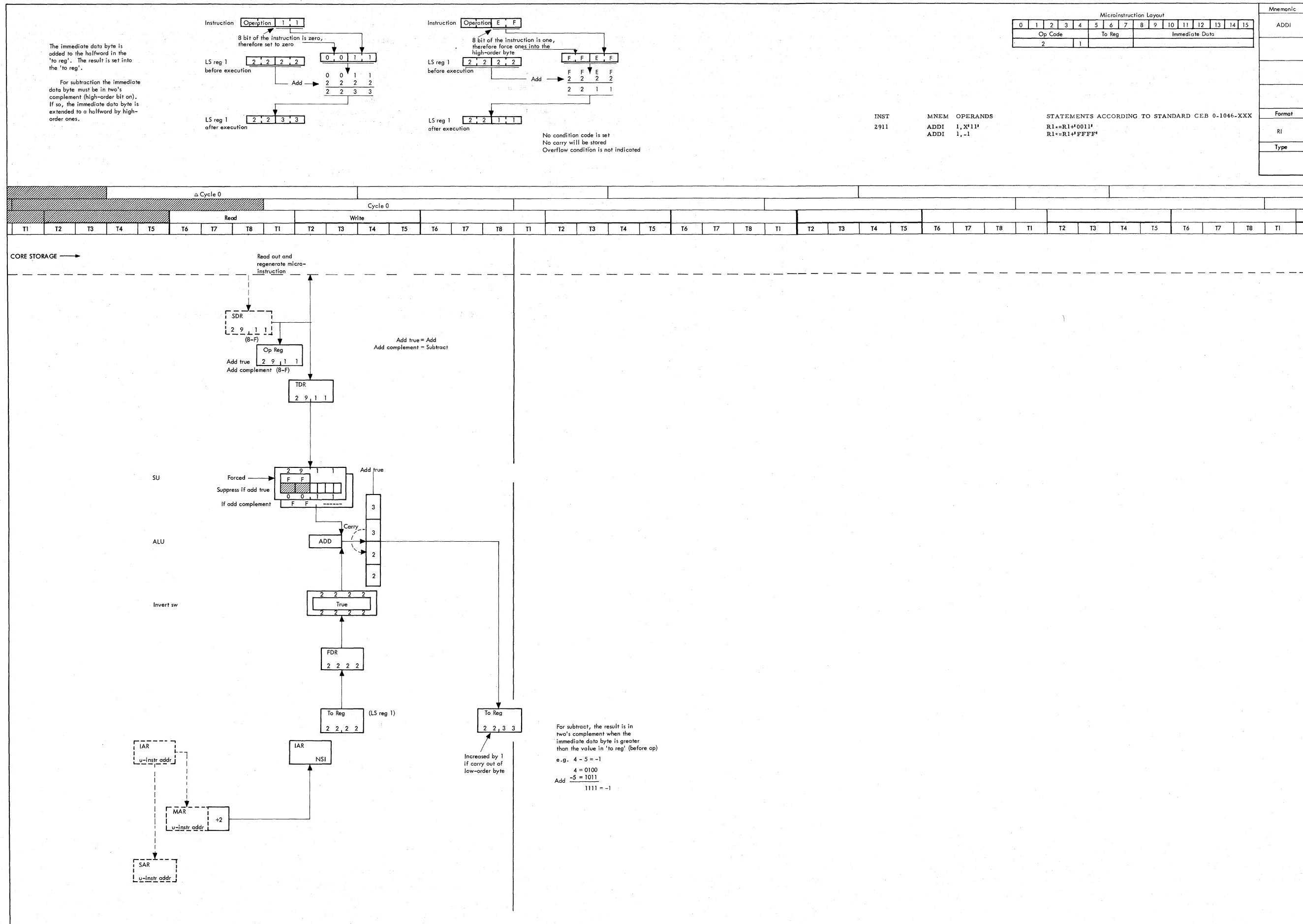


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

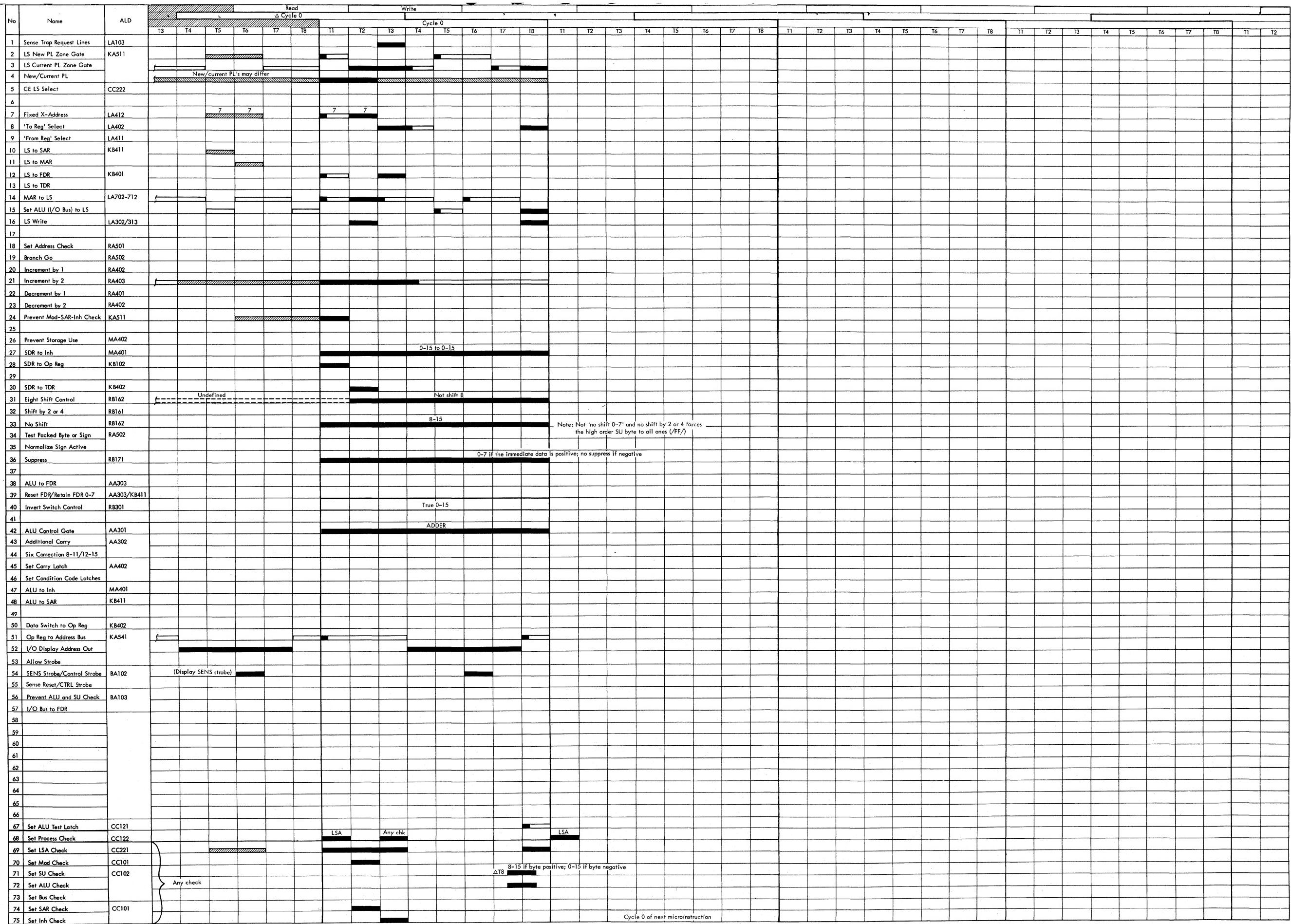
"Do not care" signals: ΔCycle Cycle

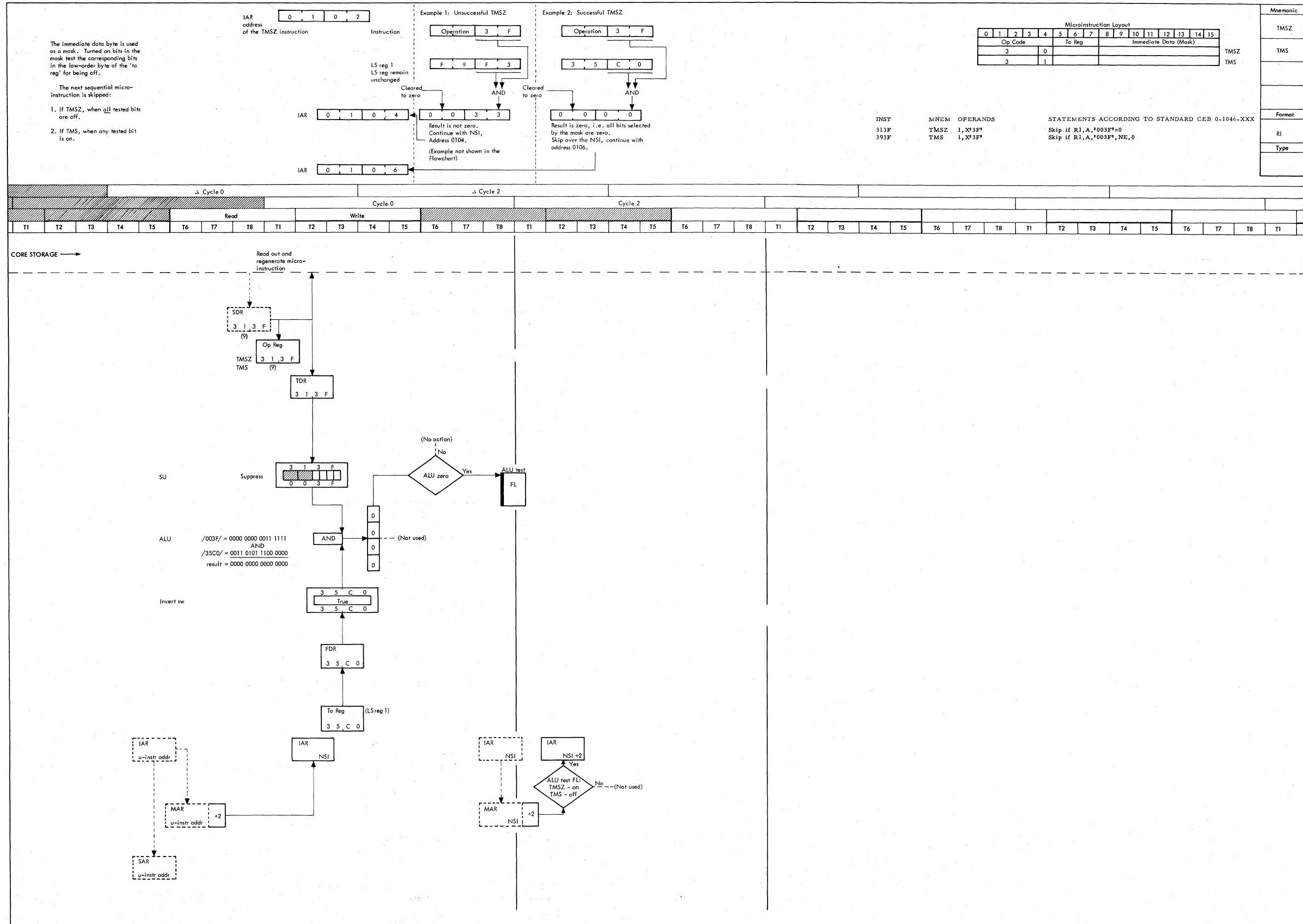


Note: For "Do not care" functions refer to timing chart below.

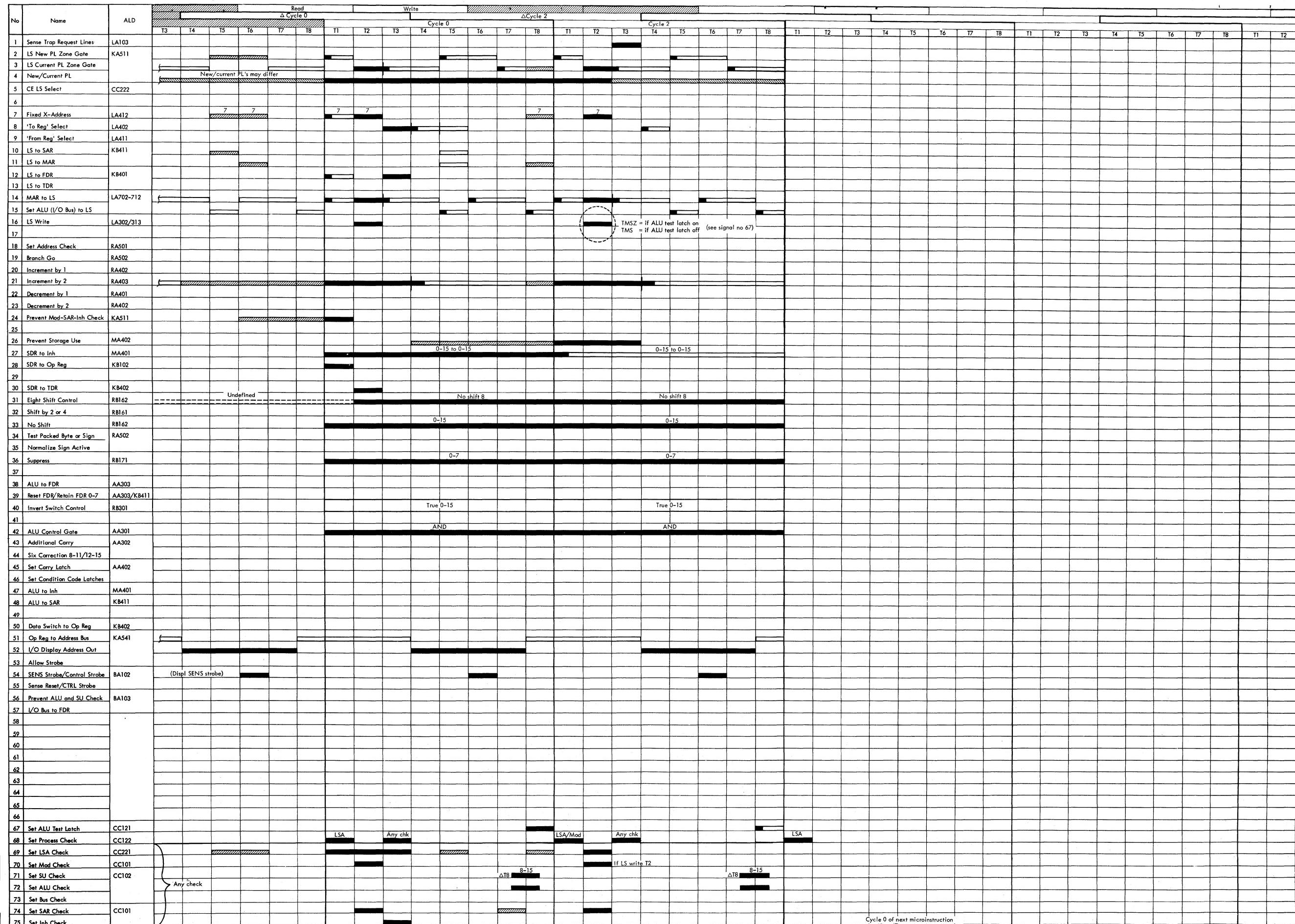
"Do not care" signals:
 Δ Cycle
 Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.





Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



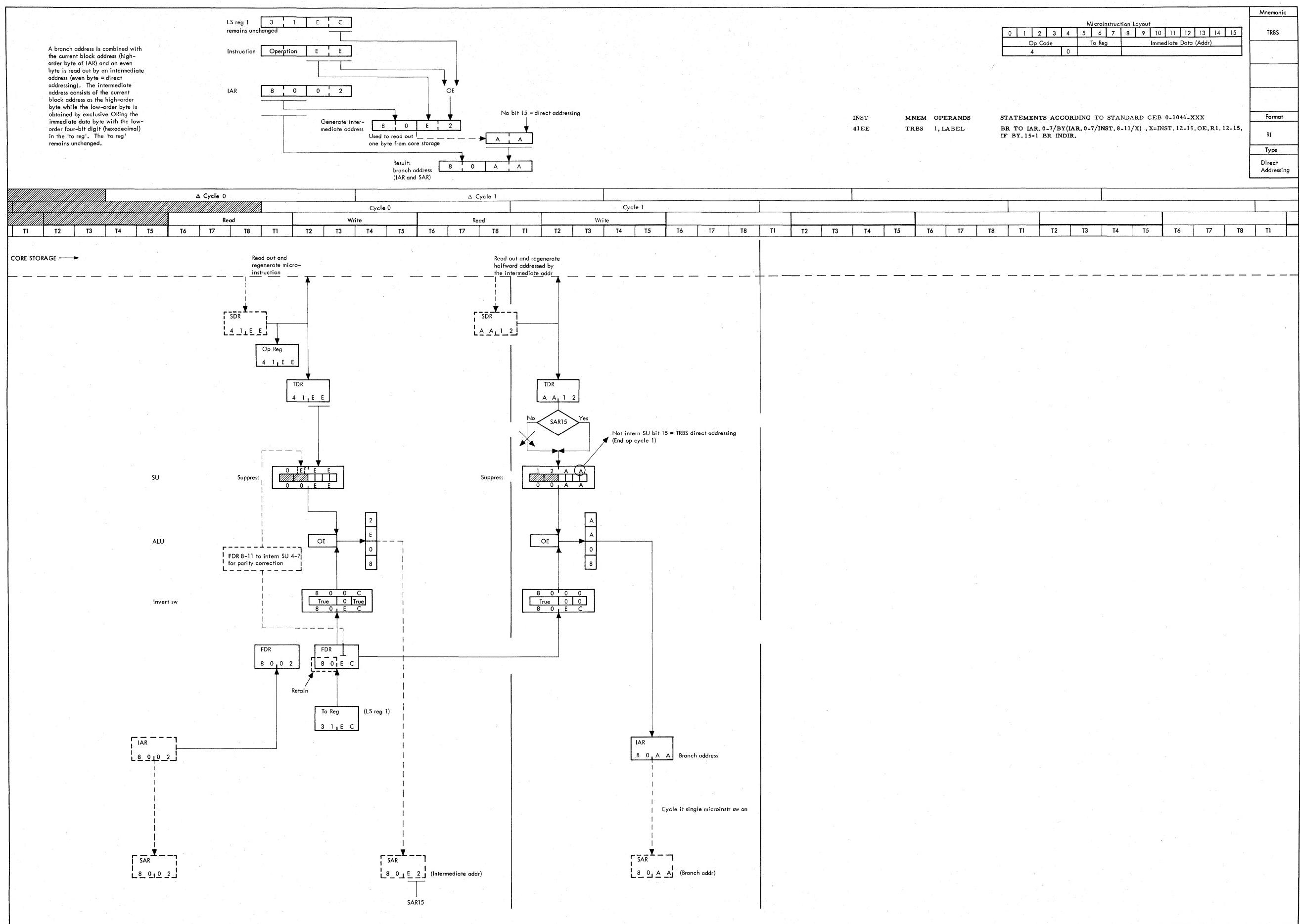
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

1

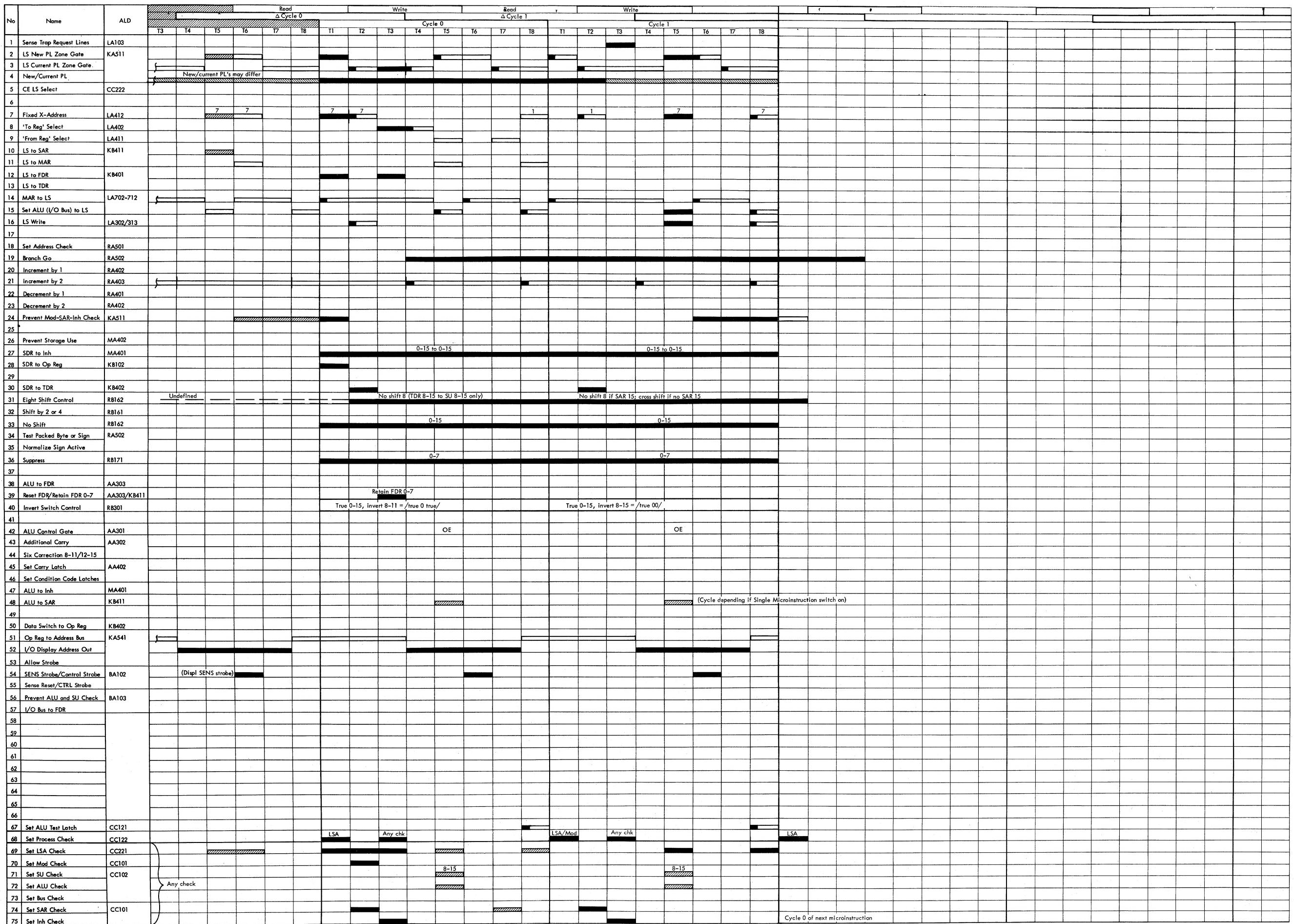
1

1

8



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

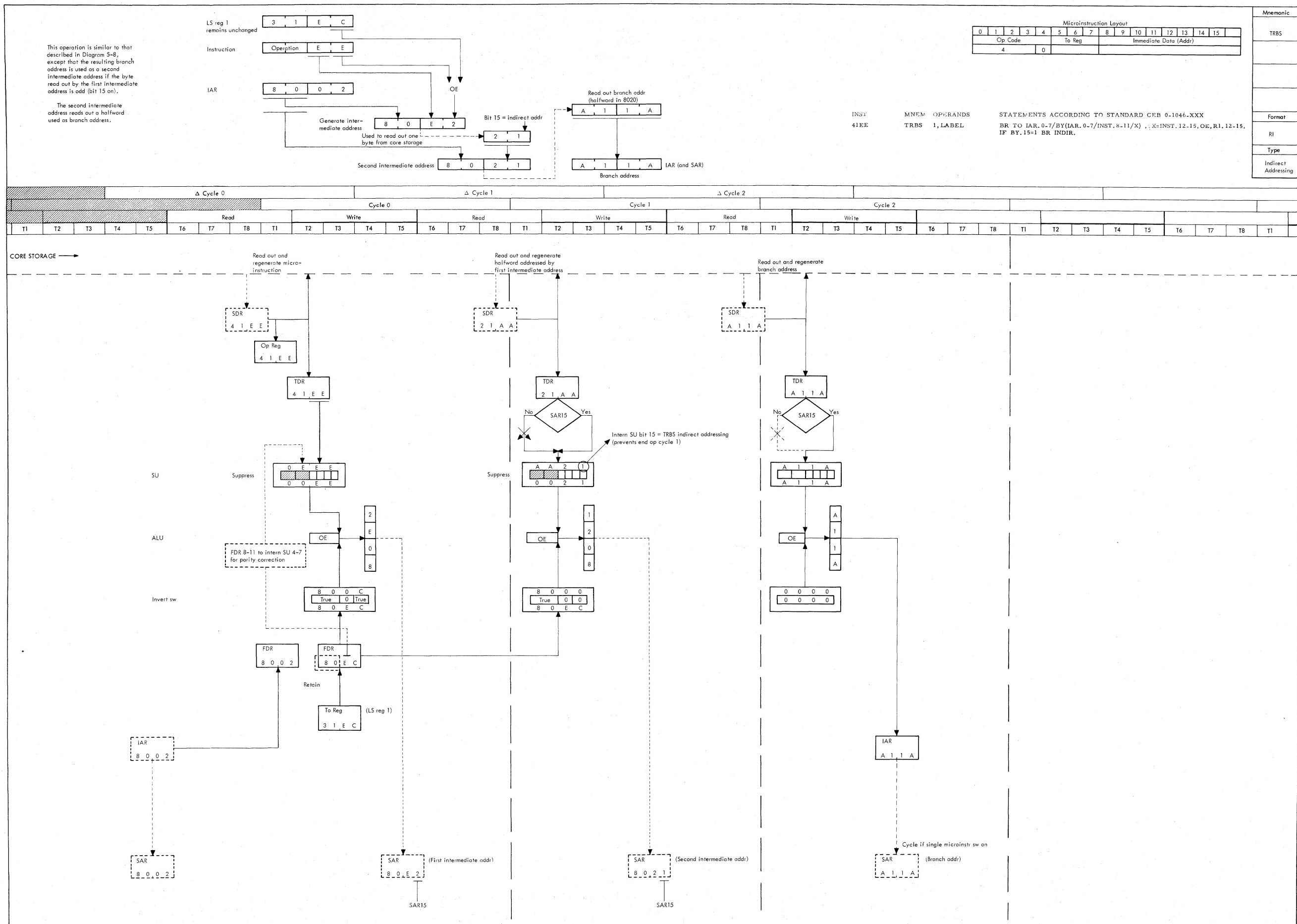
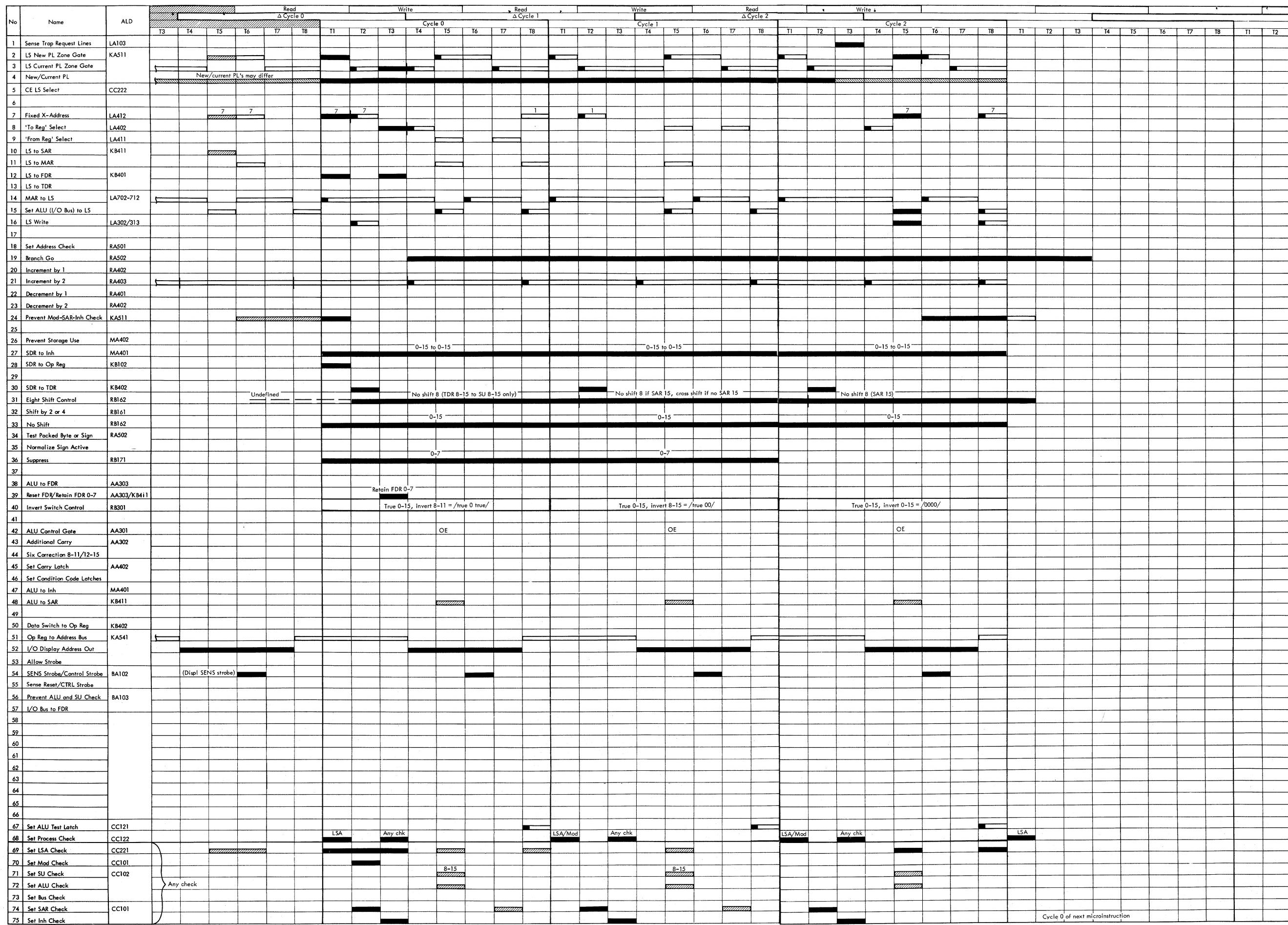
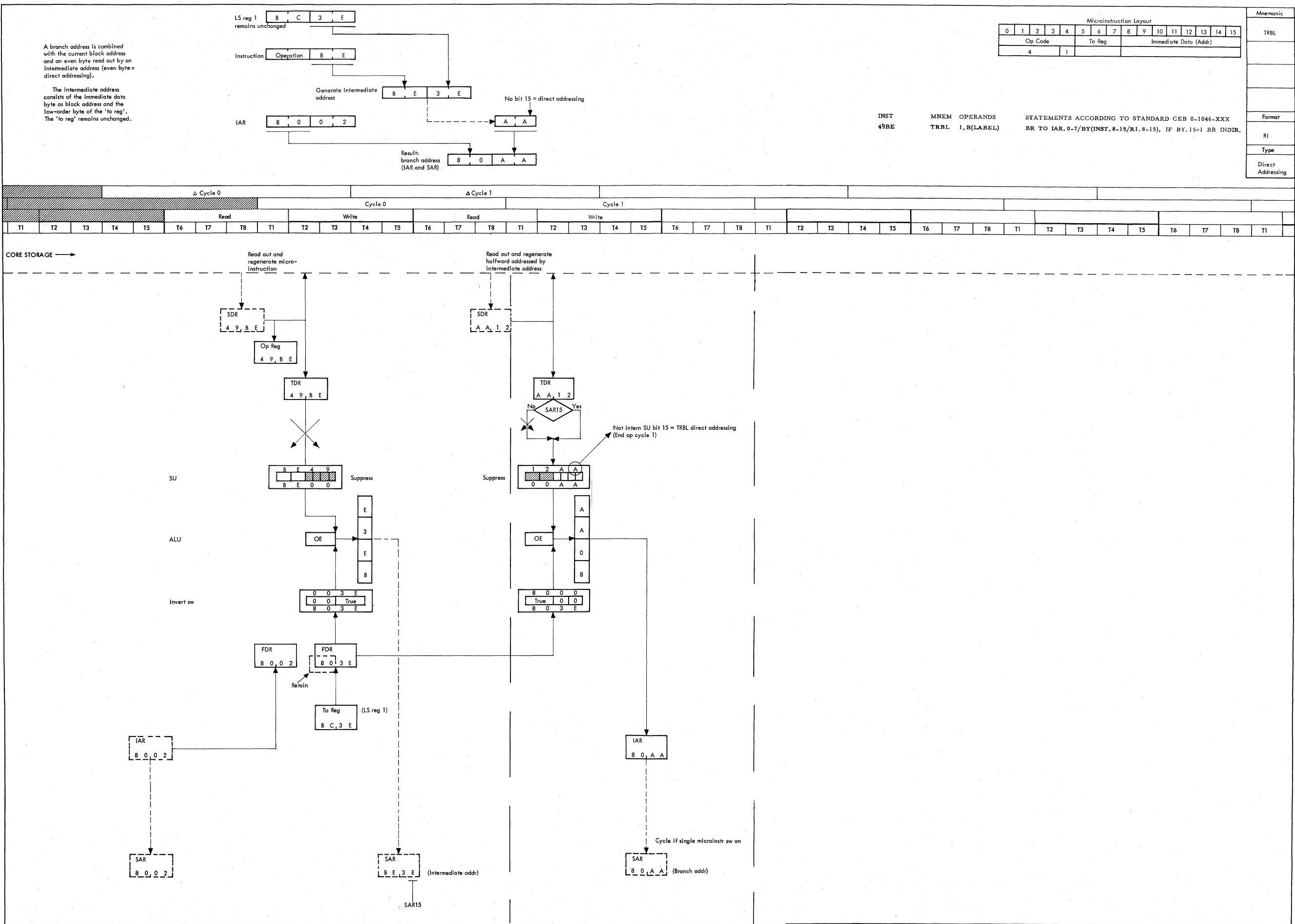


Diagram 5-9. Translate and Branch Short (Indirect Addressing) (Part 1 of 2) (03714)



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

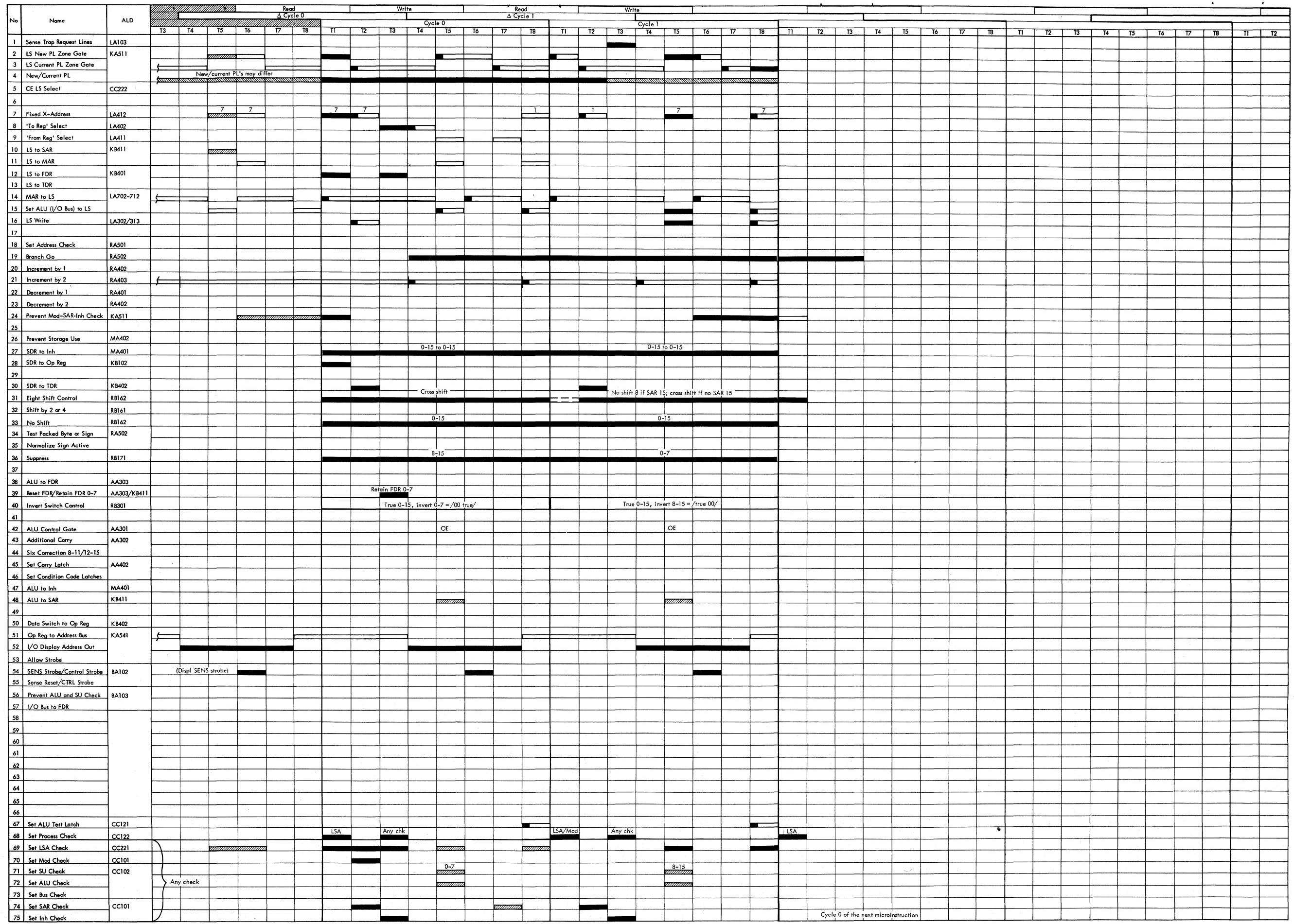
"Do not care" signals: Δ Cycle Cycle



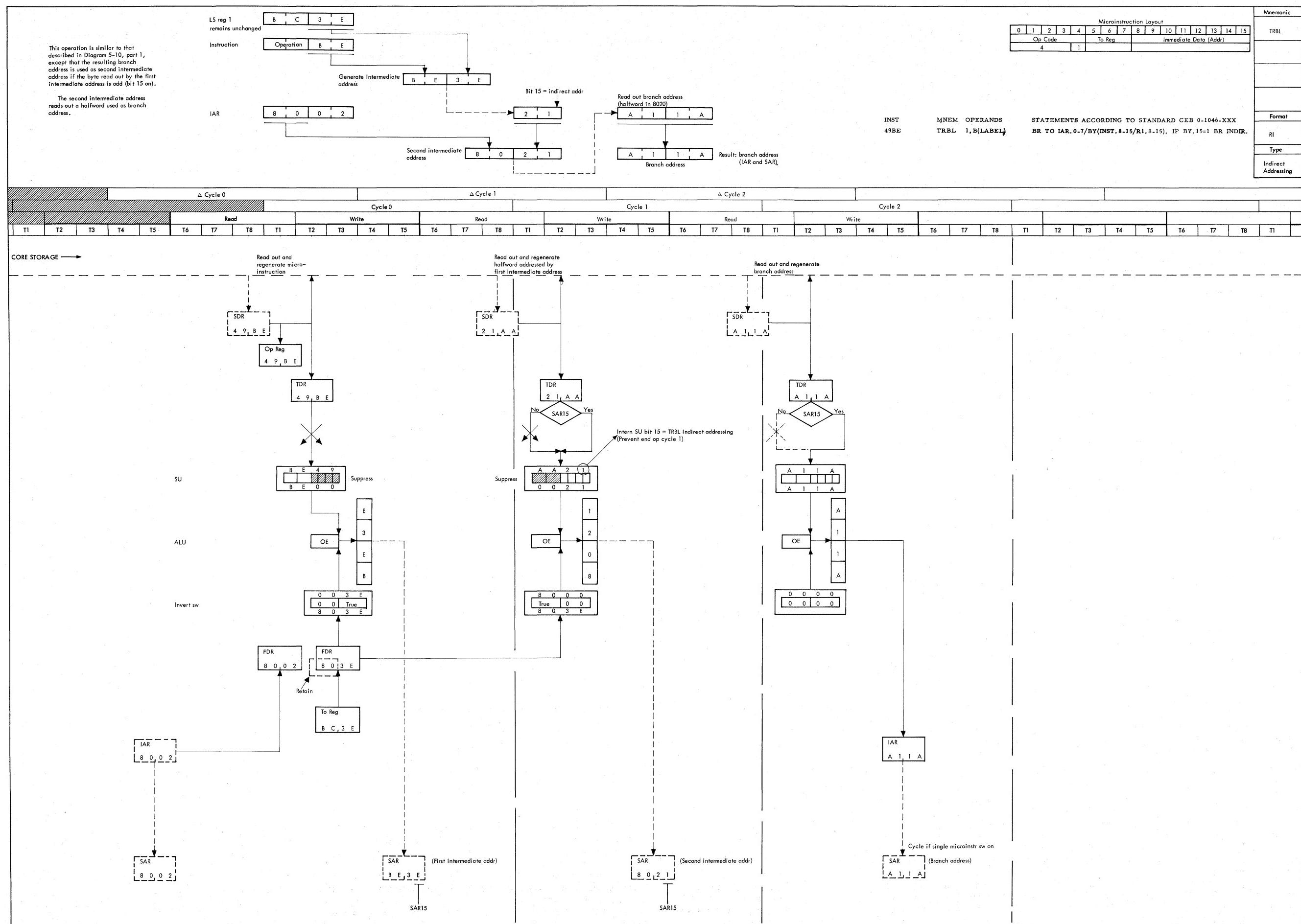
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:

ΔCycle
Cycle



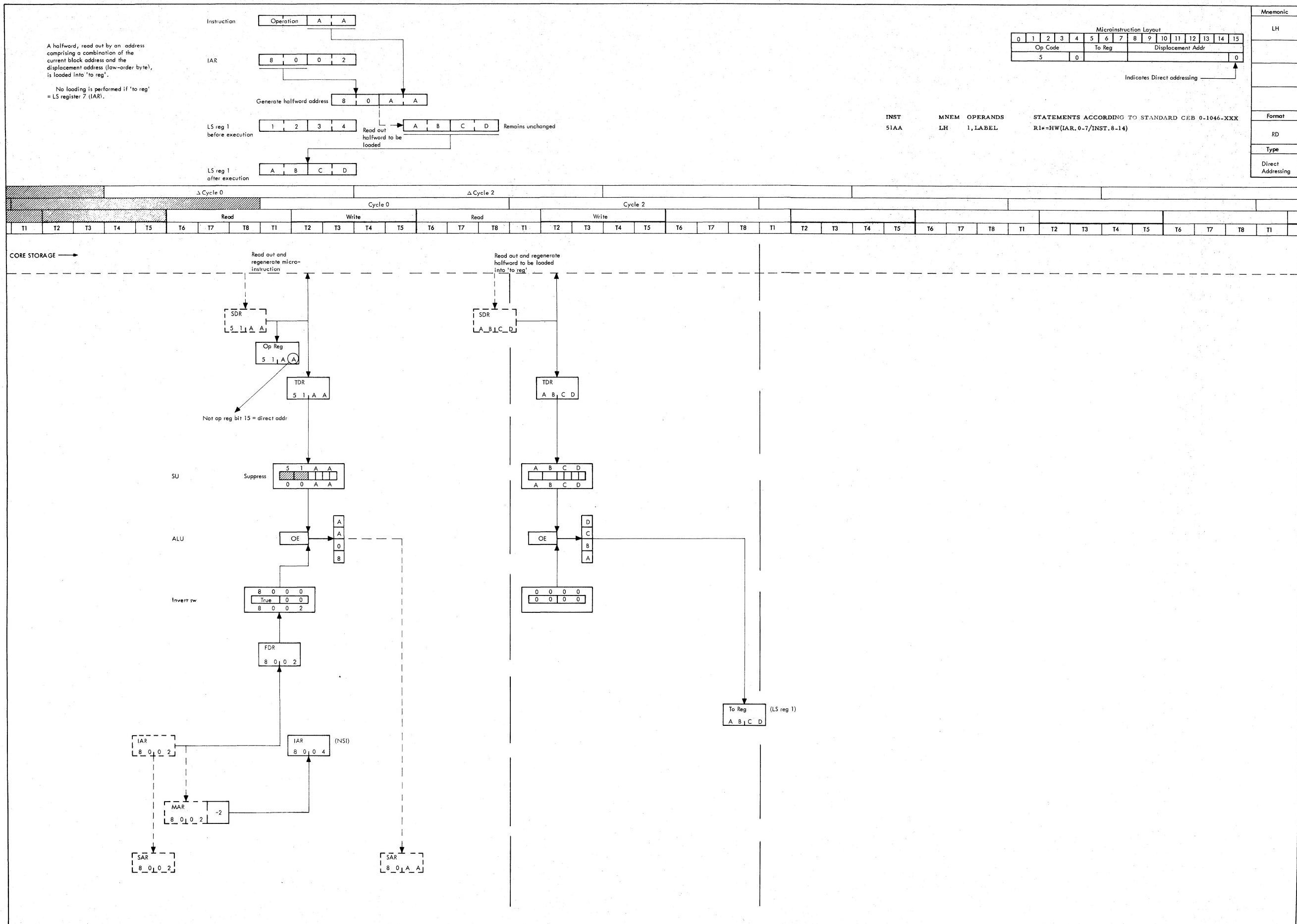
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-11. Translate and Branch Long (Indirect Addressing) (Part 1 of 2) (03716A) 2020 ≥ 50,000 FEMDM Vol-2 (8/69) •

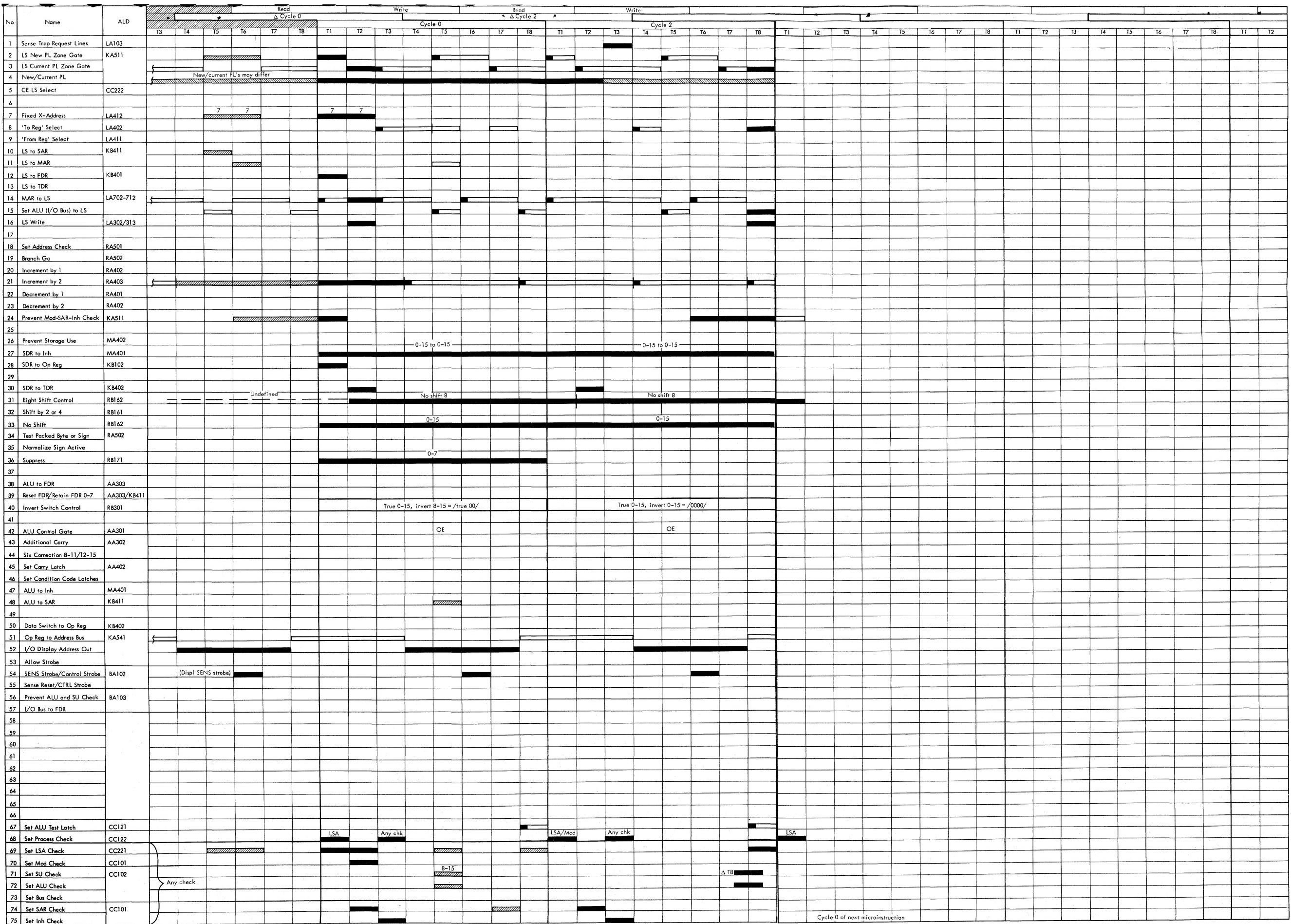
No	Name	ALD	Read Δ Cycle 0								Write								Read Δ Cycle 1								Write								Read Δ Cycle 2								Write	
			T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T1	T2								
1	Sense Trap Request Lines	LA103																																										
2	LS New PL Zone Gate	KA511																																										
3	LS Current PL Zone Gate																																											
4	New/Current PL		New/current PL's may differ																																									
5	CE LS Select	CC222																																										
6																																												
7	Fixed X-Address	LA412	7	7						7	7								1		1																							
8	'To Reg' Select	LA402																																										
9	'From Reg' Select	LA411																																										
10	LS to SAR	KB411																																										
11	LS to MAR																																											
12	LS to FDR	KB401																																										
13	LS to TDR																																											
14	MAR to LS	LA702-712																																										
15	Set ALU (I/O Bus) to LS																																											
16	LS Write	LA302/313																																										
17																																												
18	Set Address Check	RA501																																										
19	Branch Go	RA502																																										
20	Increment by 1	RA402																																										
21	Increment by 2	RA403																																										
22	Decrement by 1	RA401																																										
23	Decrement by 2	RA402																																										
24	Prevent Mod-SAR-Inh Check	KA511																																										
25																																												
26	Prevent Storage Use	MA402																																										
27	SDR to Inh	MA401																																										
28	SDR to Op Reg	KB102																																										
29																																												
30	SDR to TDR	KB402																																										
31	Eight Shift Control	RB162																																										
32	Shift by 2 or 4	RB161																																										
33	No Shift	RB162																																										
34	Test Packed Byte or Sign	RA502																																										

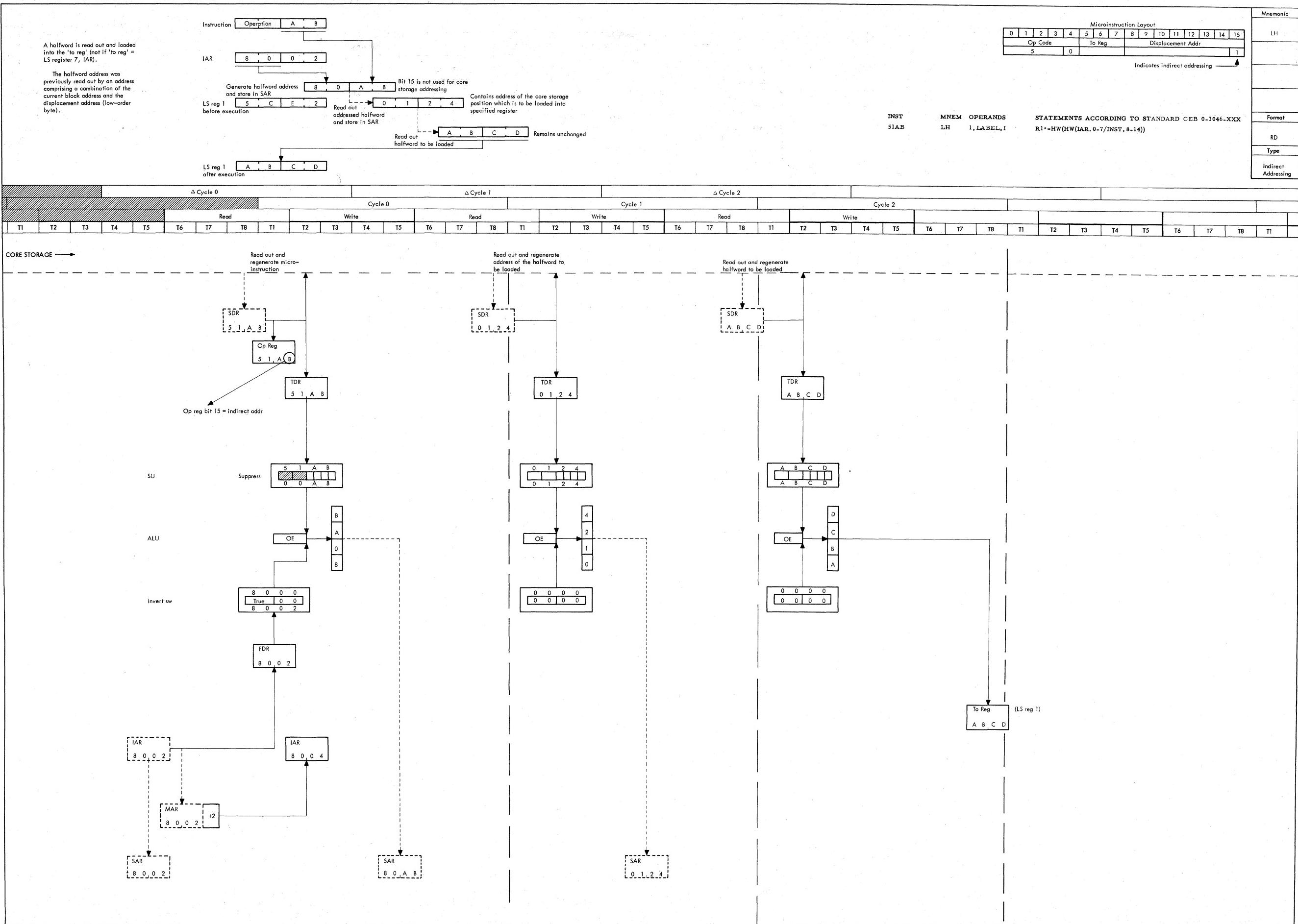


Note: For "Do not care" functions refer to timing chart below.

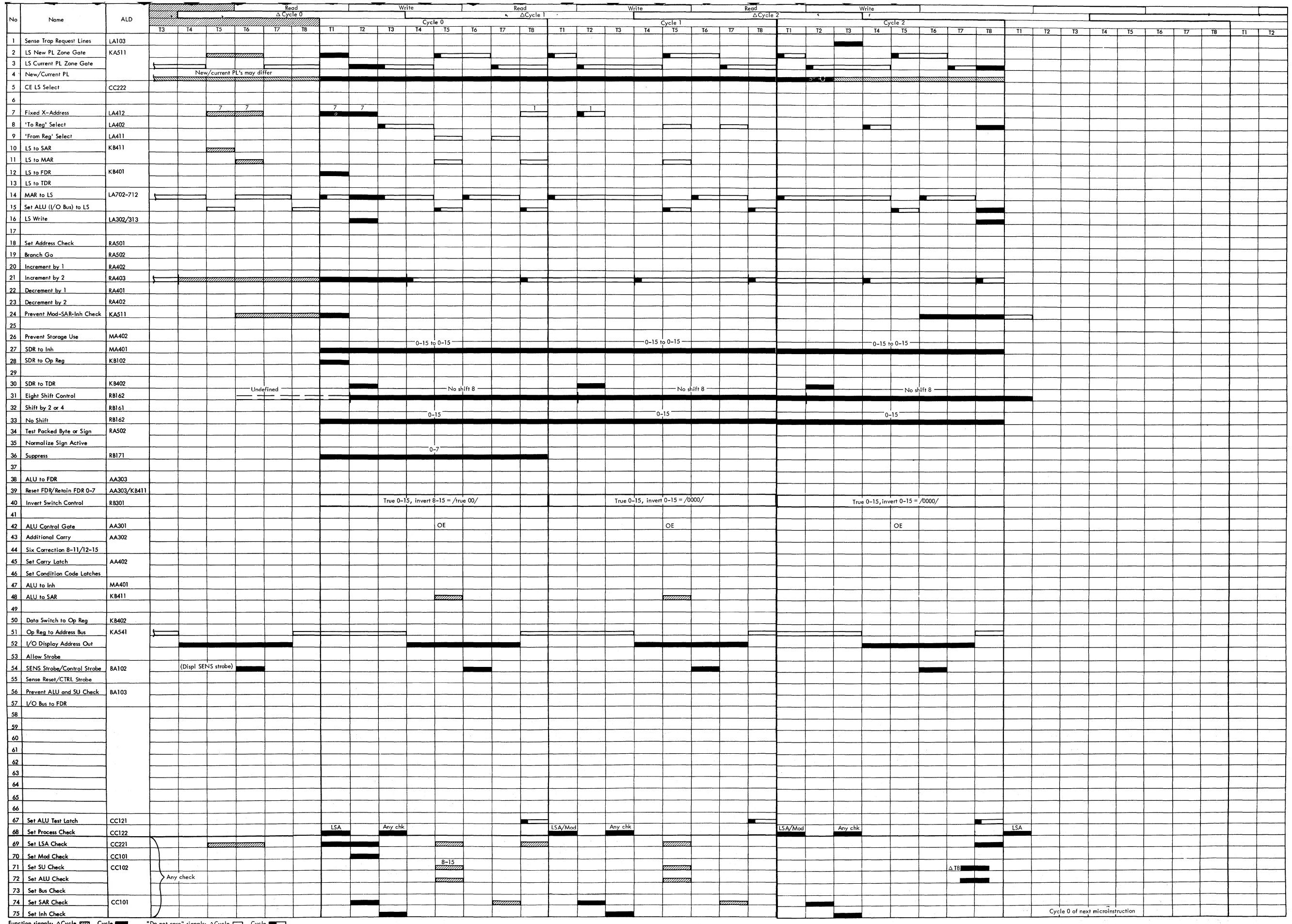
"Do not care" signals:
 Δ Cycle Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



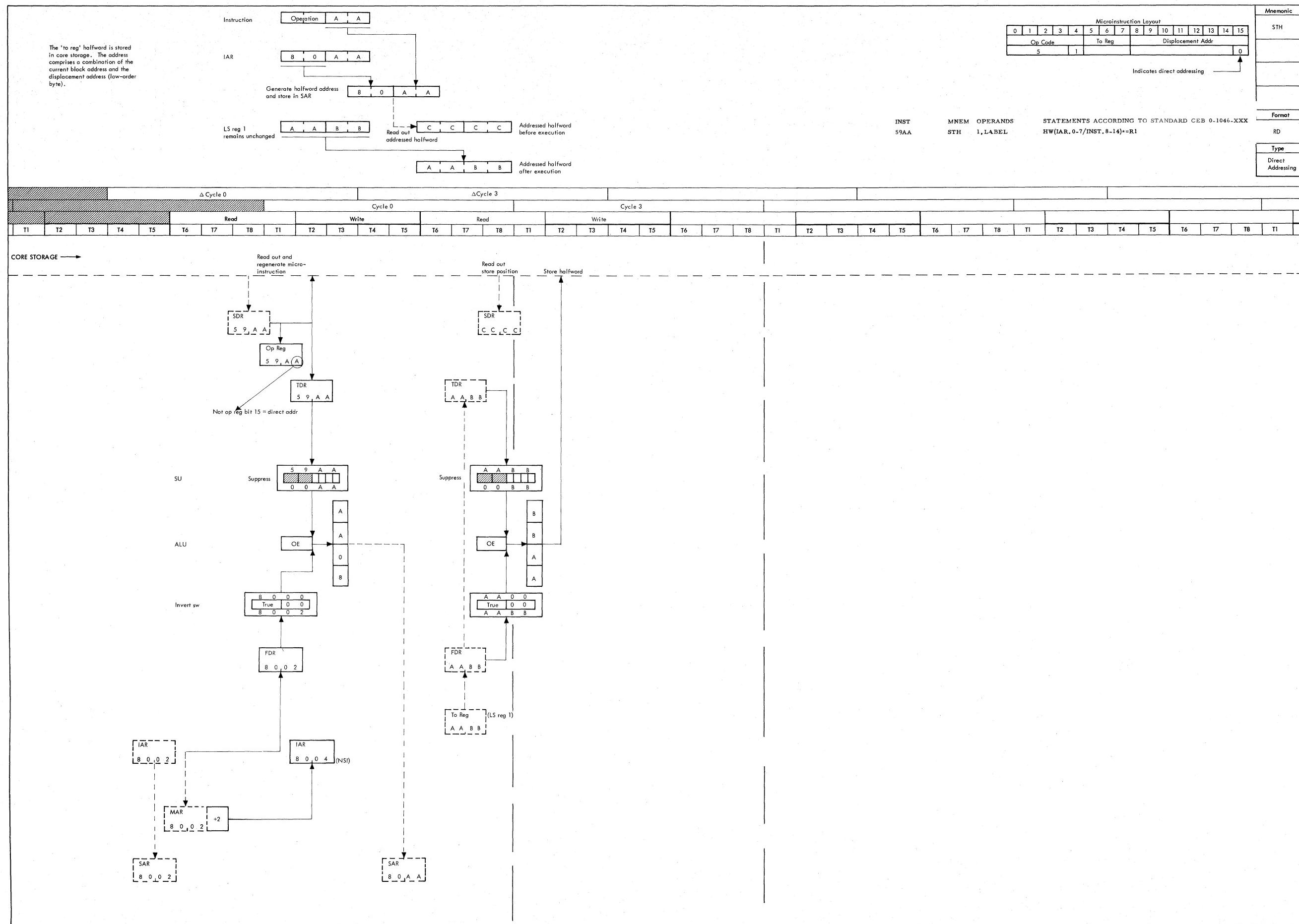


Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

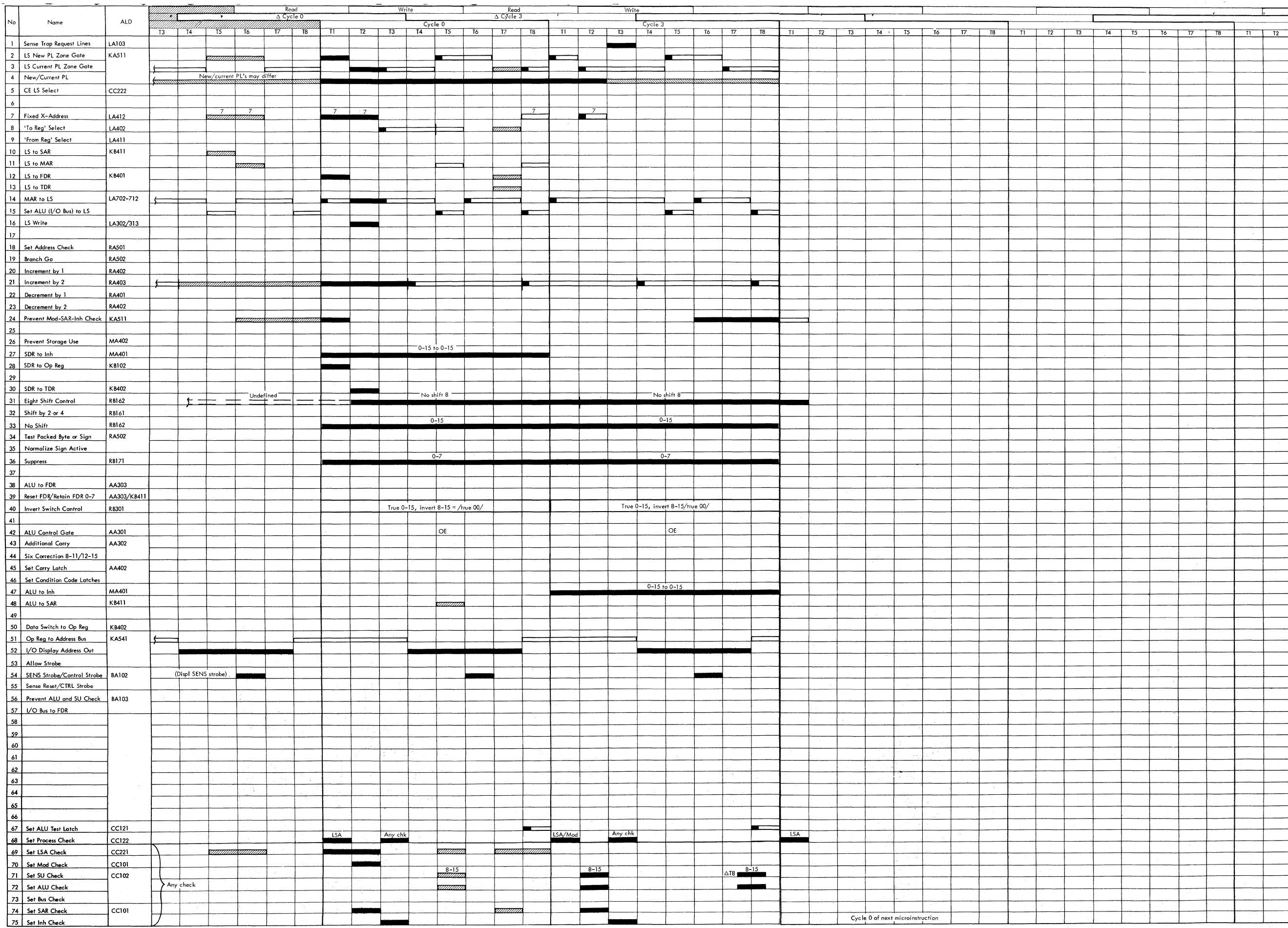


Function signals: Δ Cycle  Cycle  "Do not care" signals: Δ Cycle  Cycle 

"Do not care" signals: ΔCycle Cycle

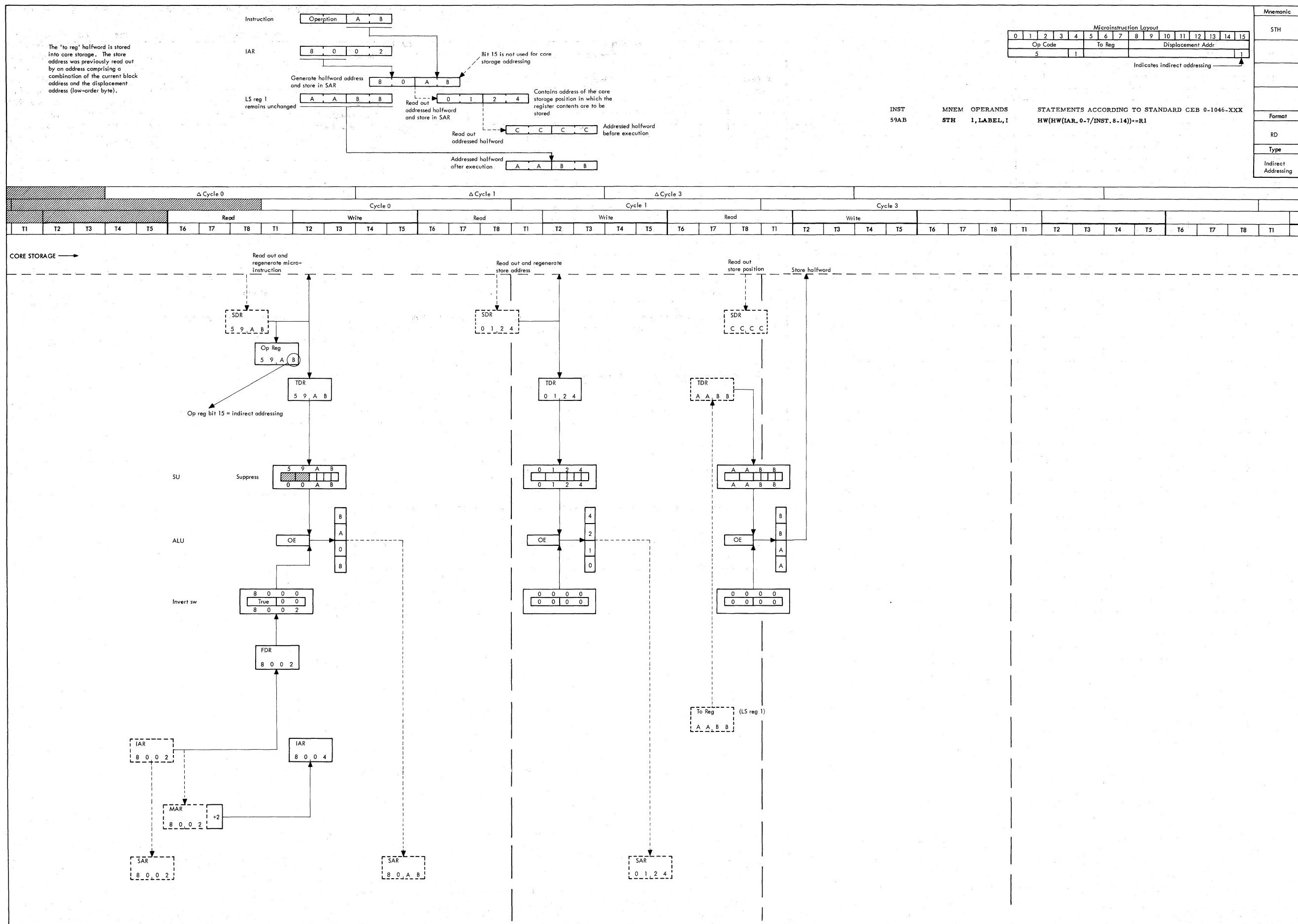


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

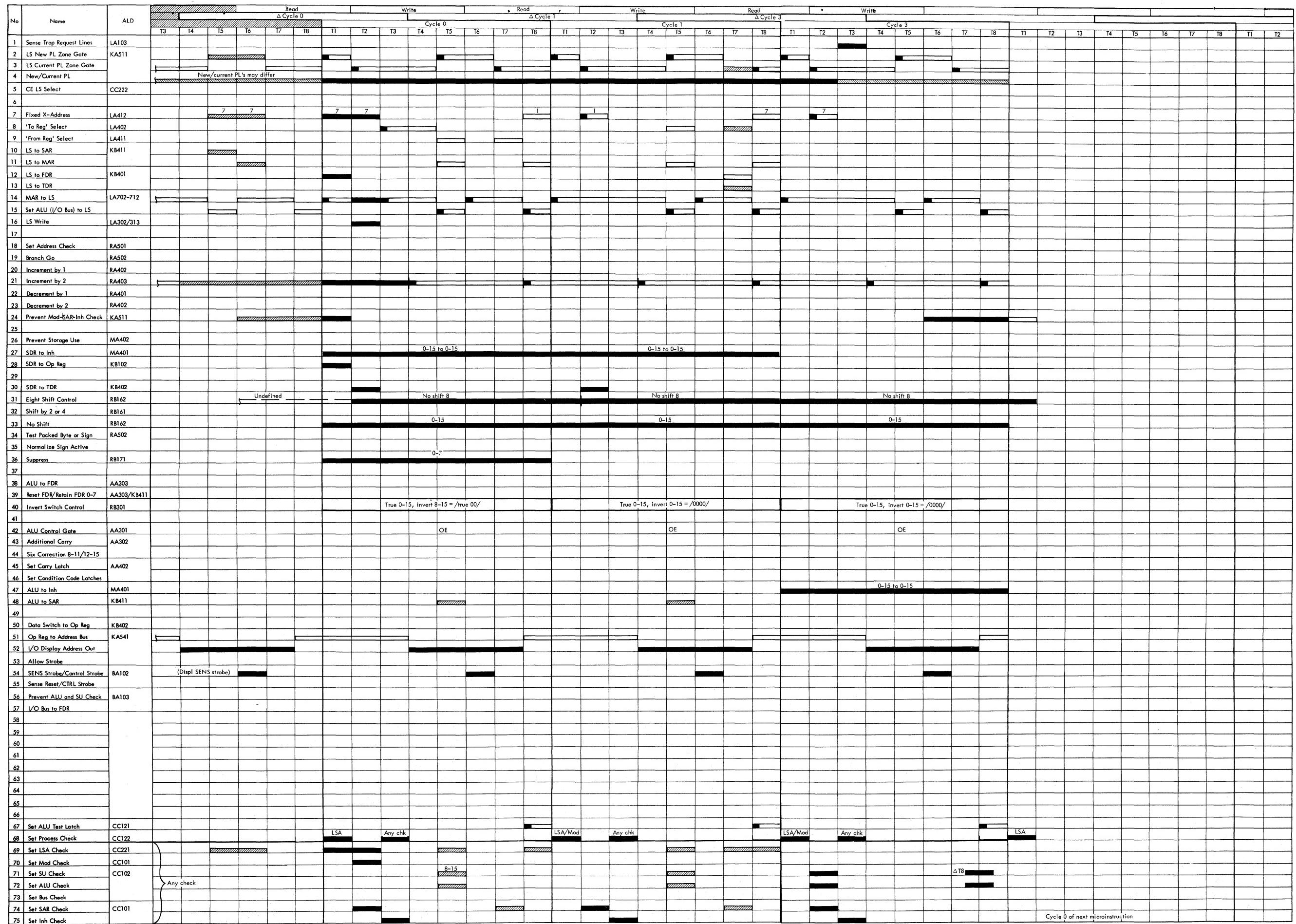


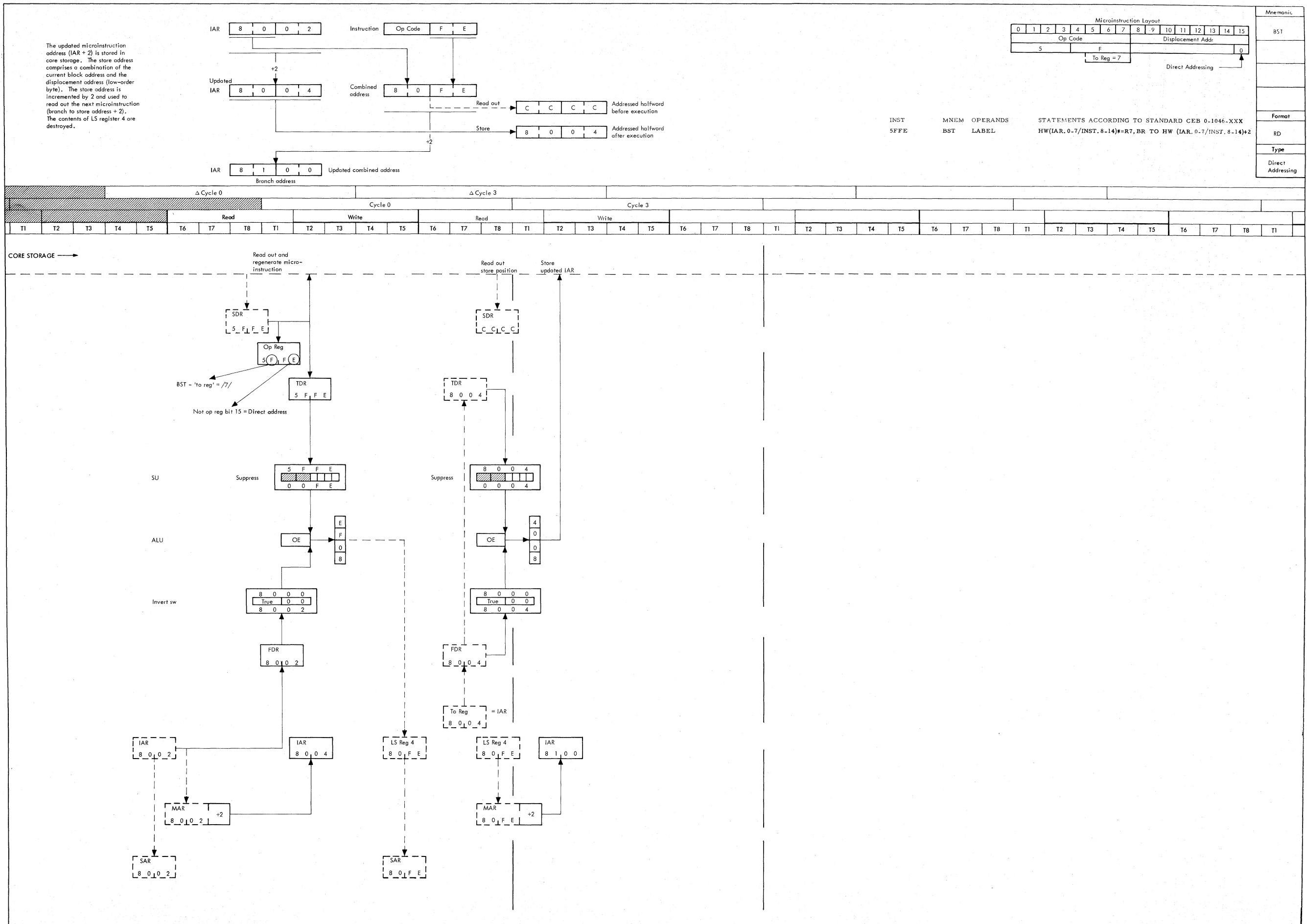
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: ΔCycle Cycle

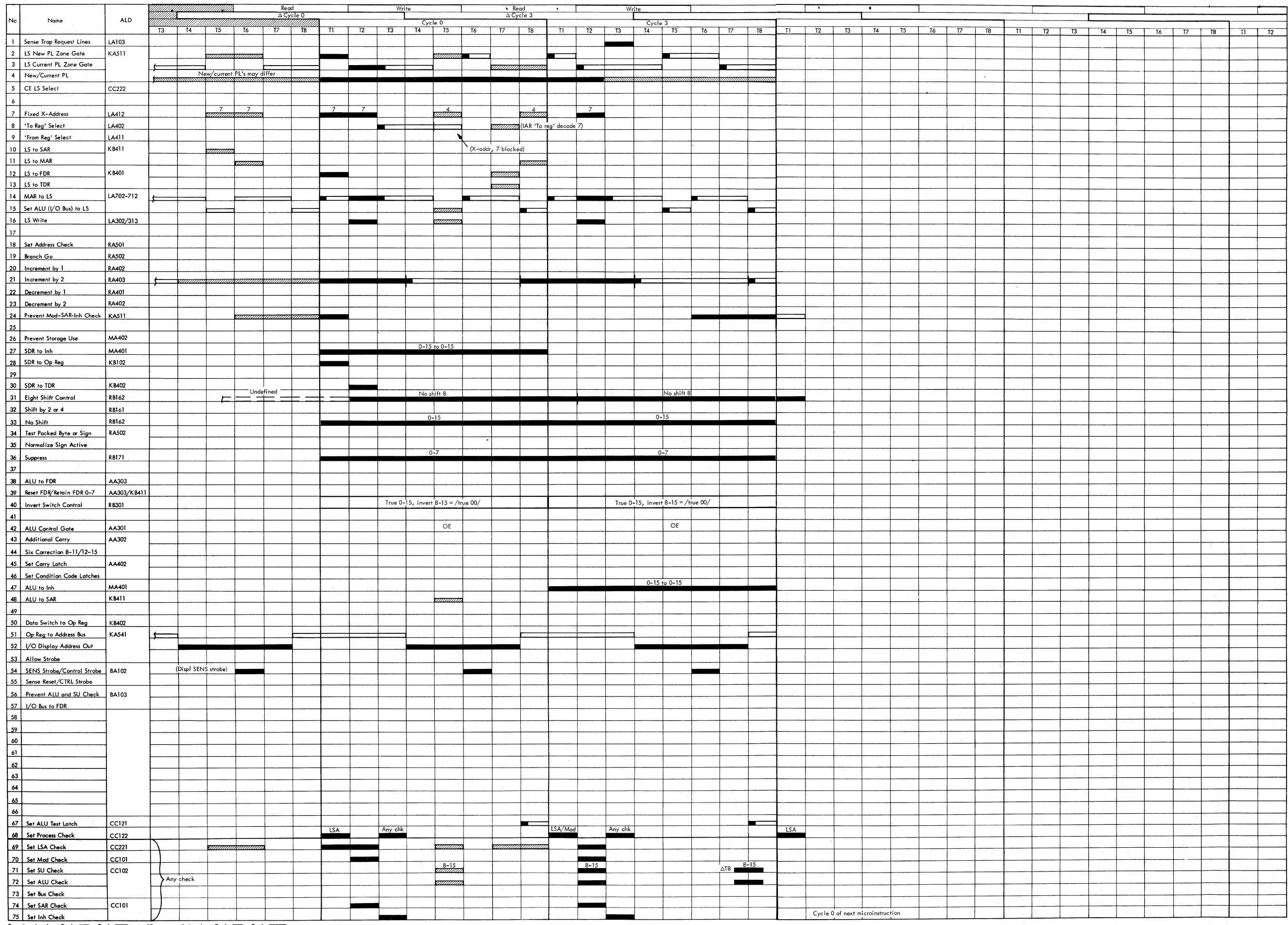


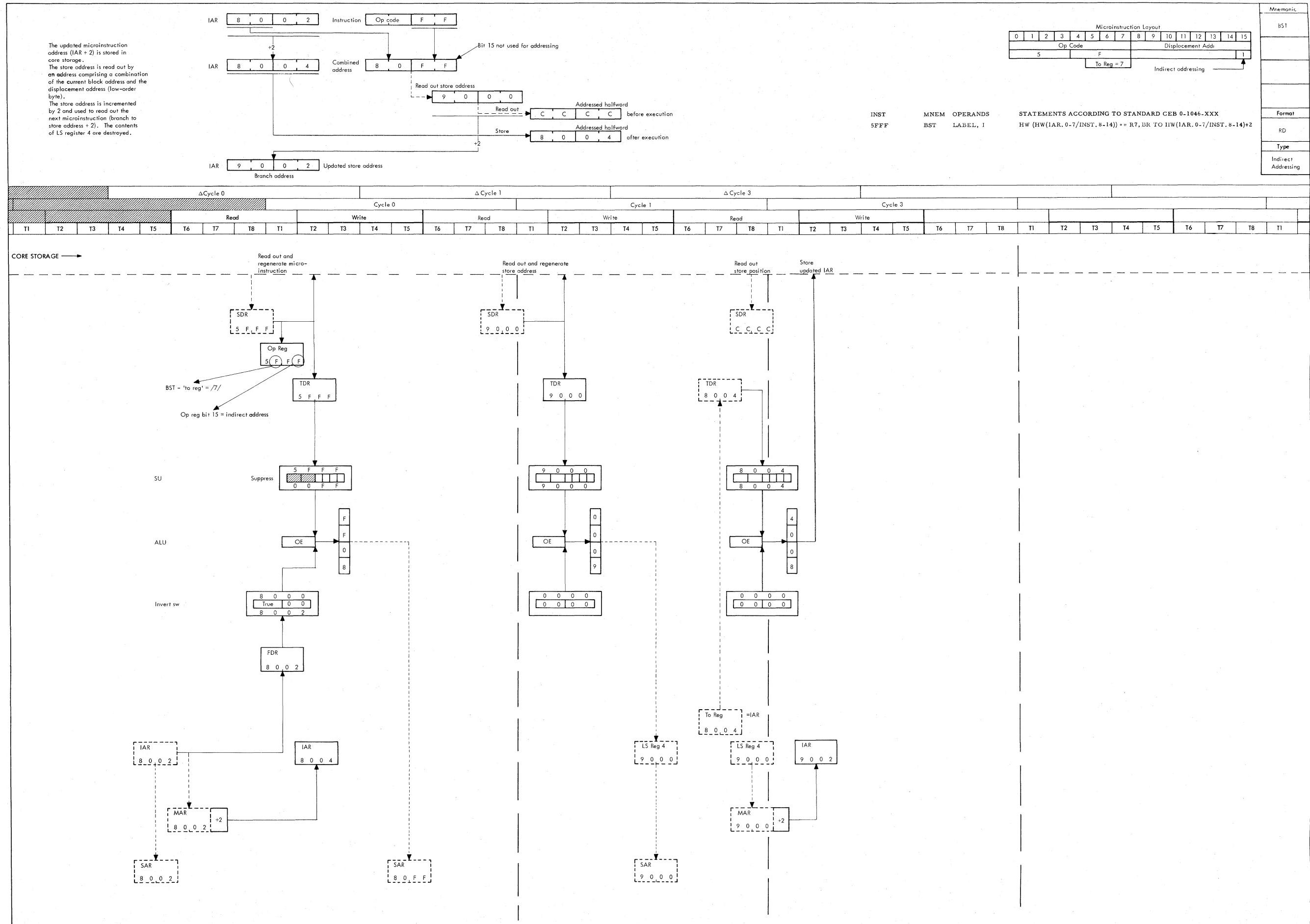
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.





Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



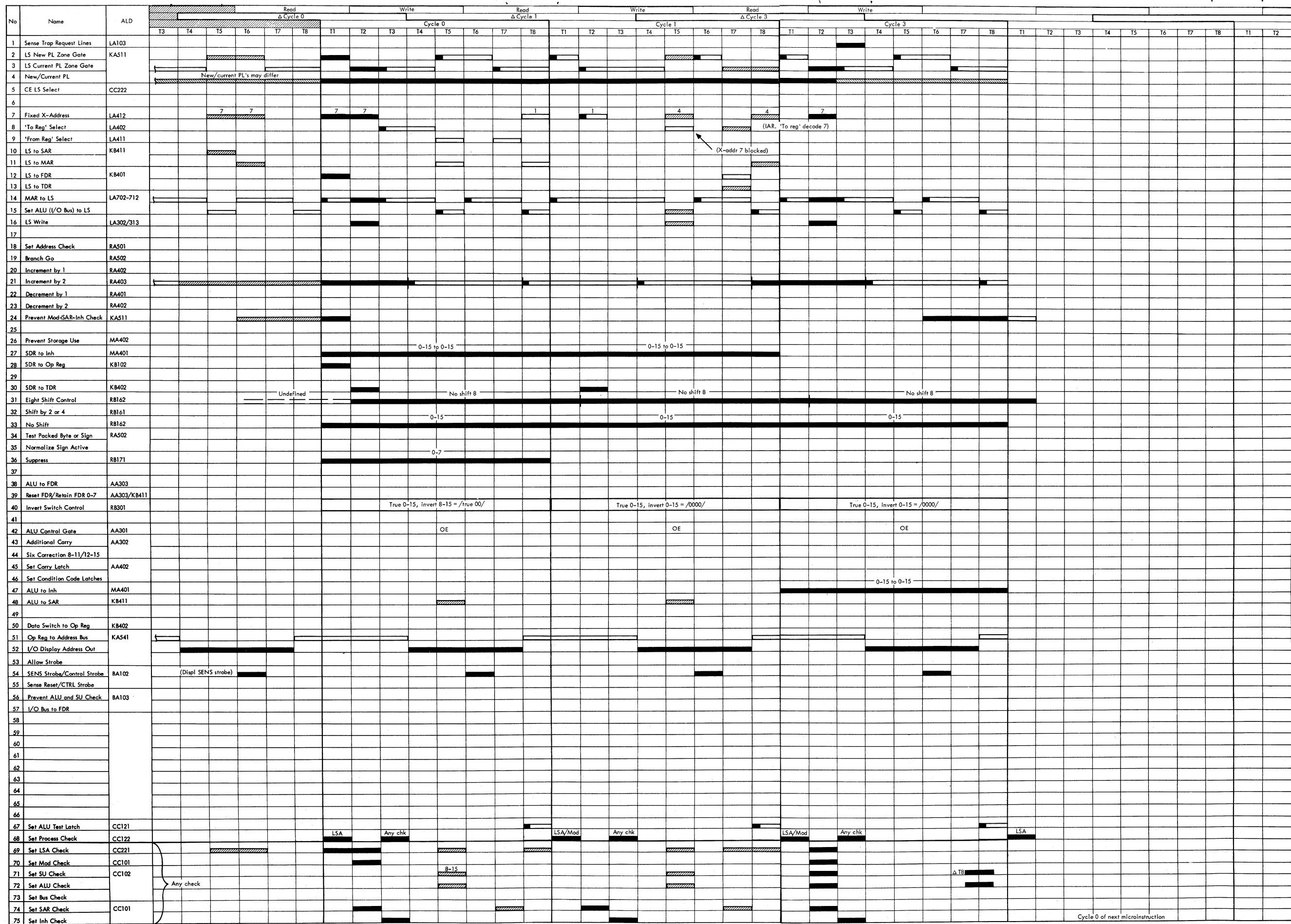


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-17. Branch and Store (Indirect Addressing) (Part 1 of 2) (03722) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

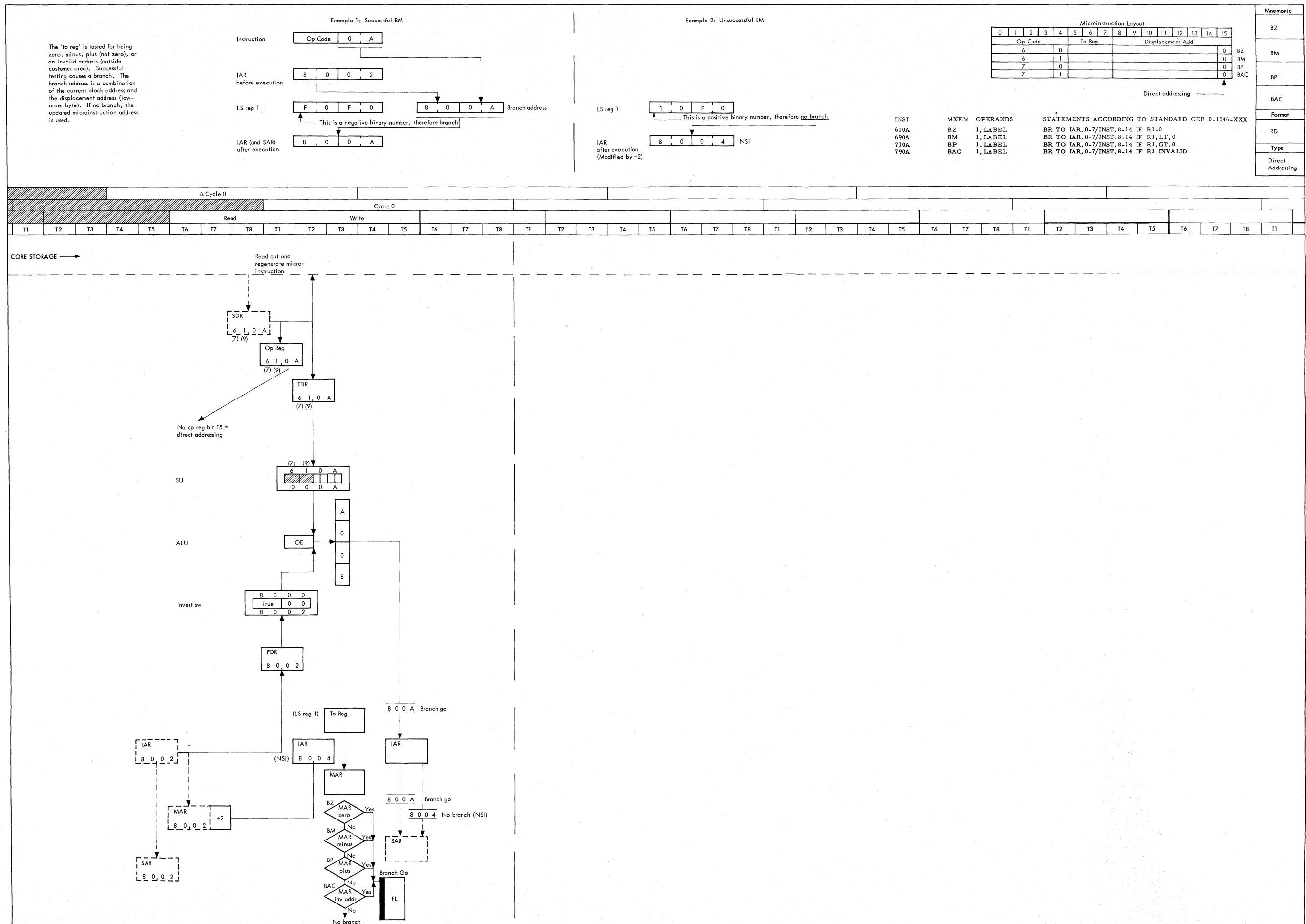
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
 ΔCycle Cycle

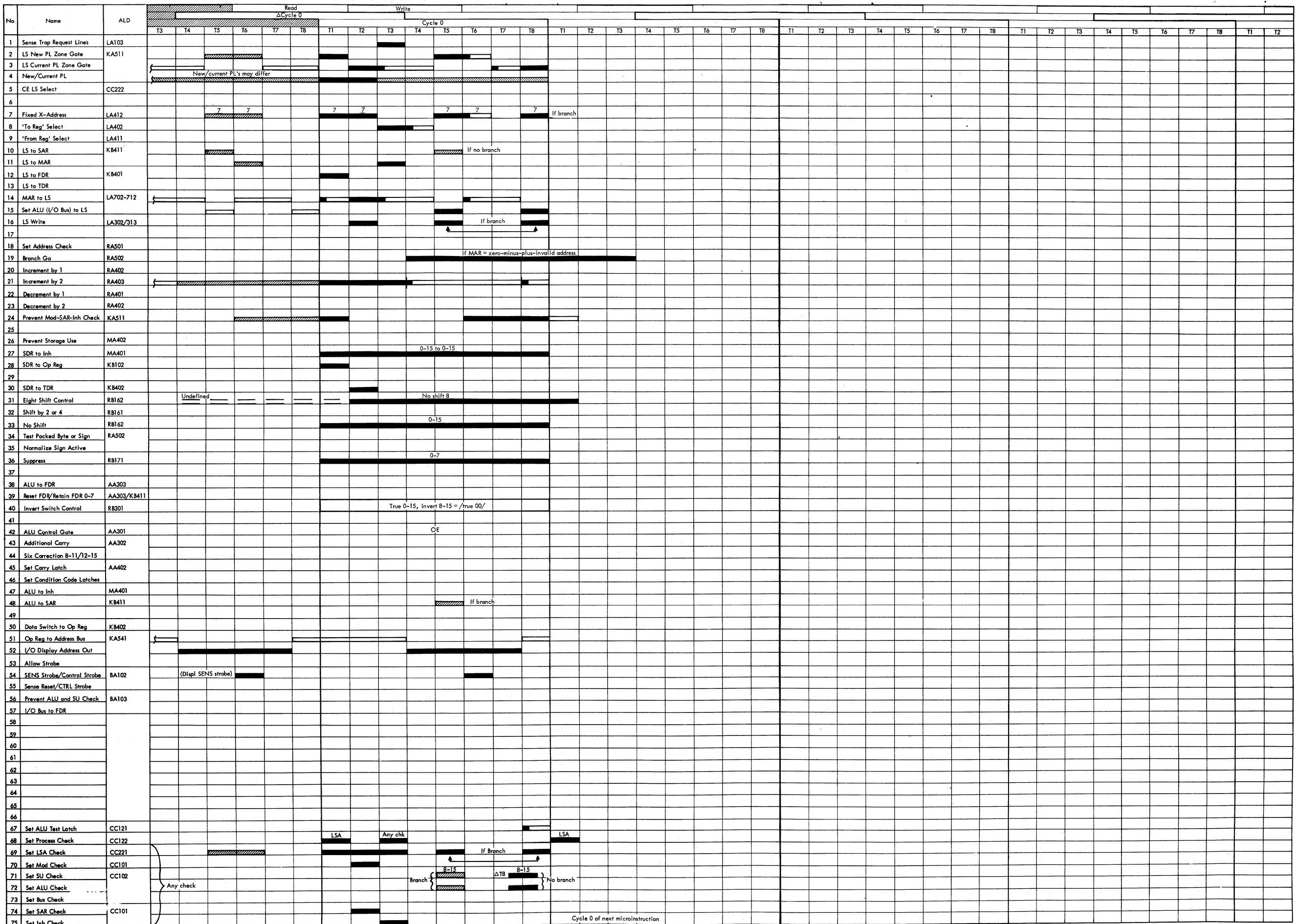


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

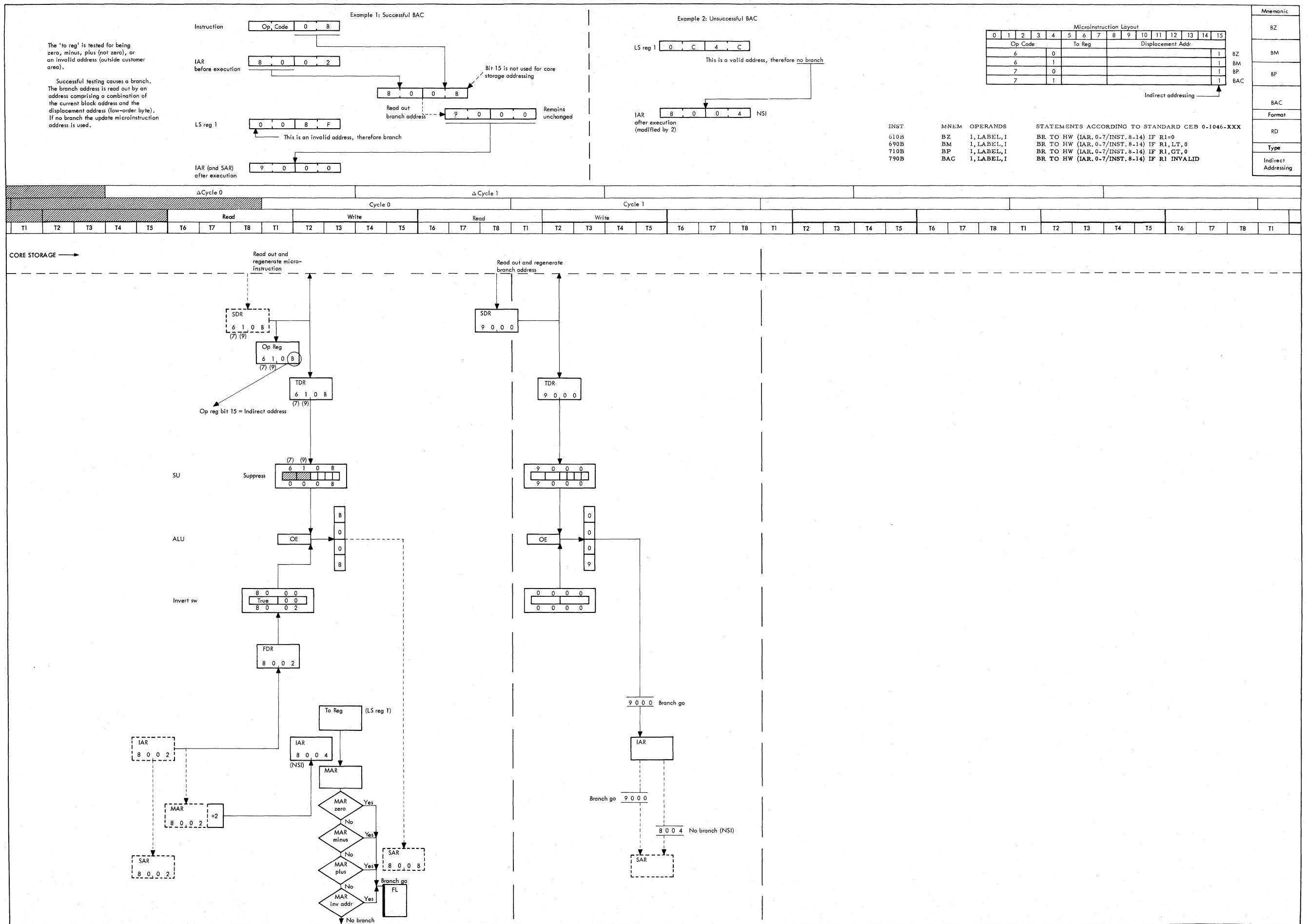


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

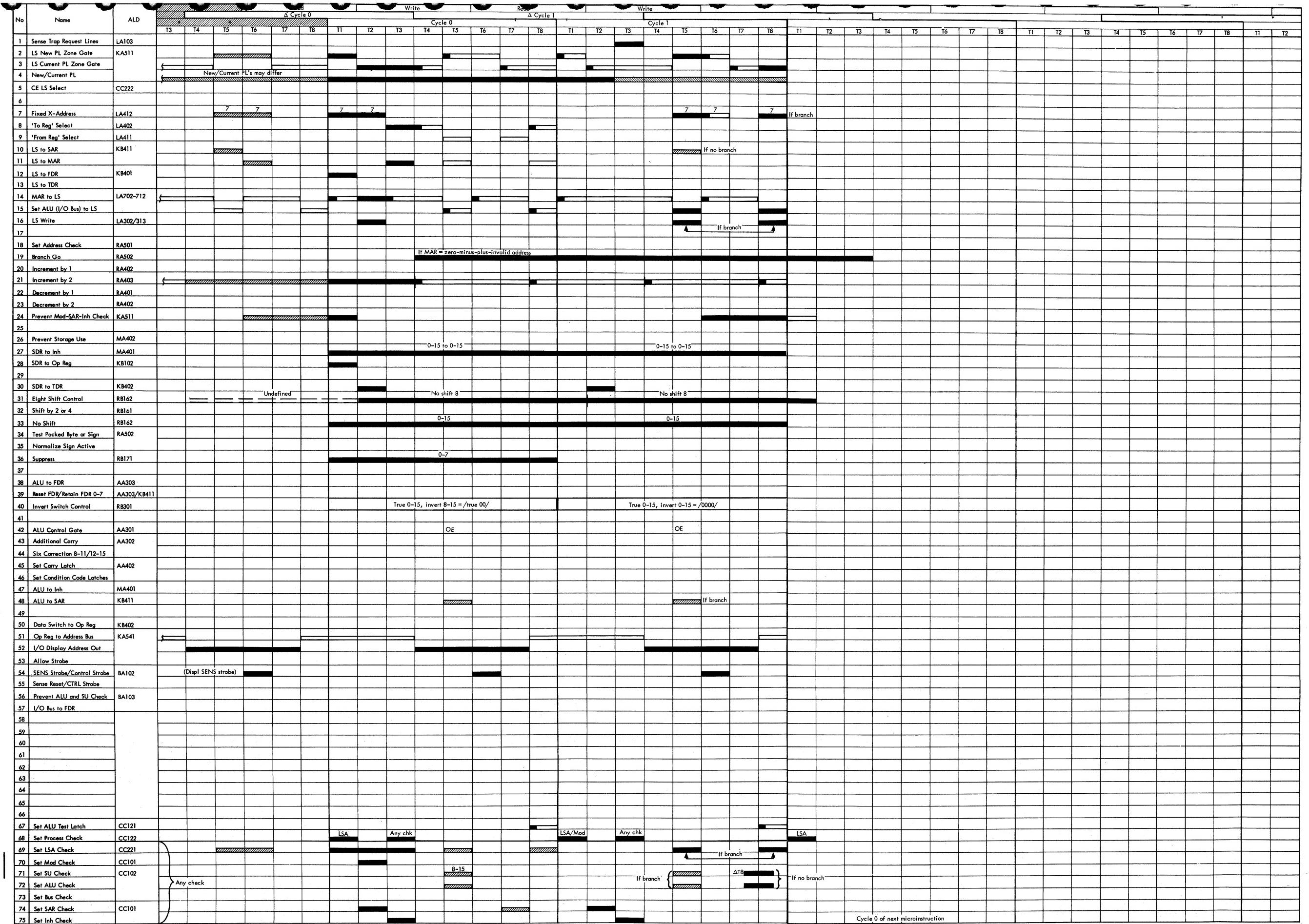


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:

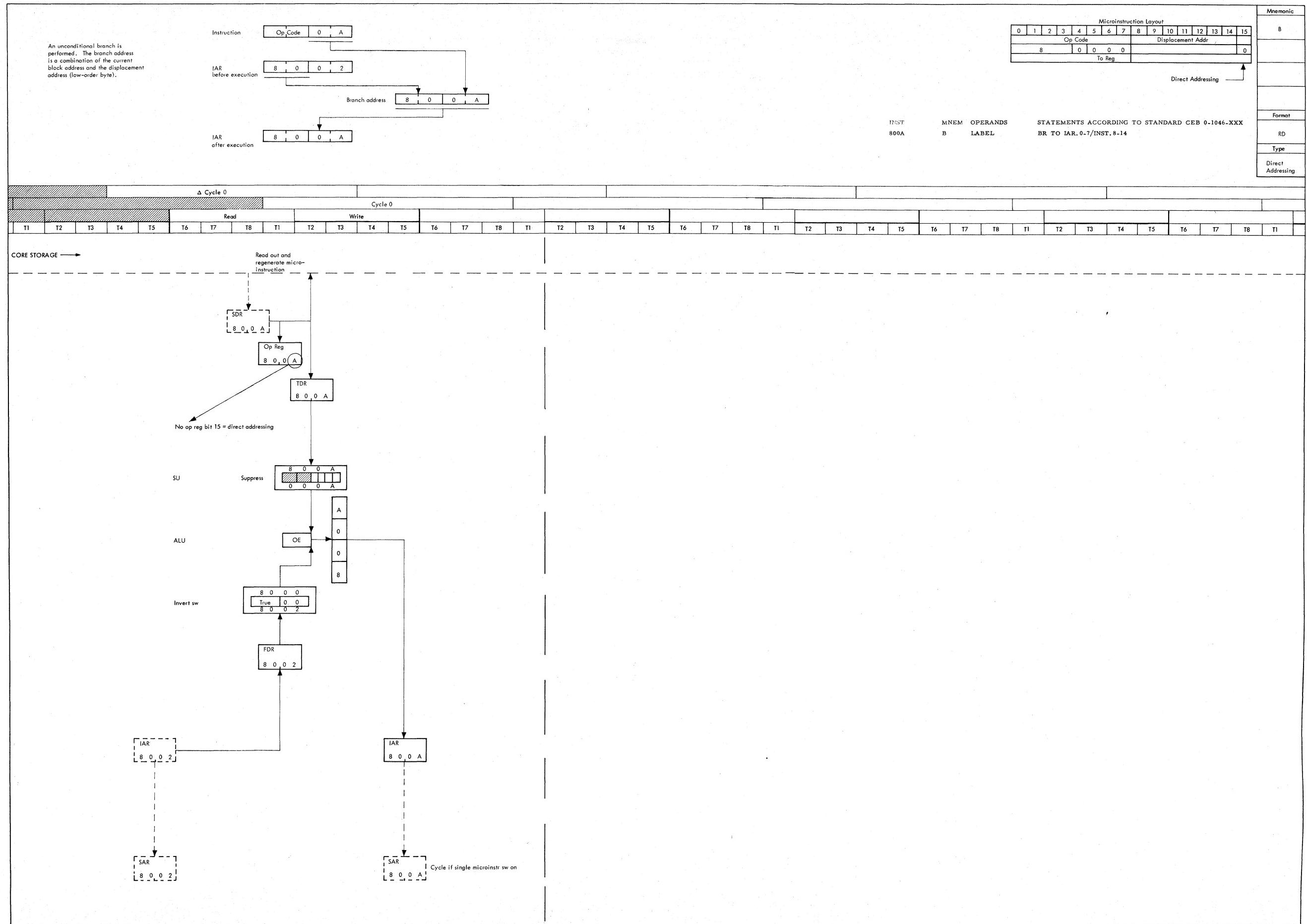
ΔCycle Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

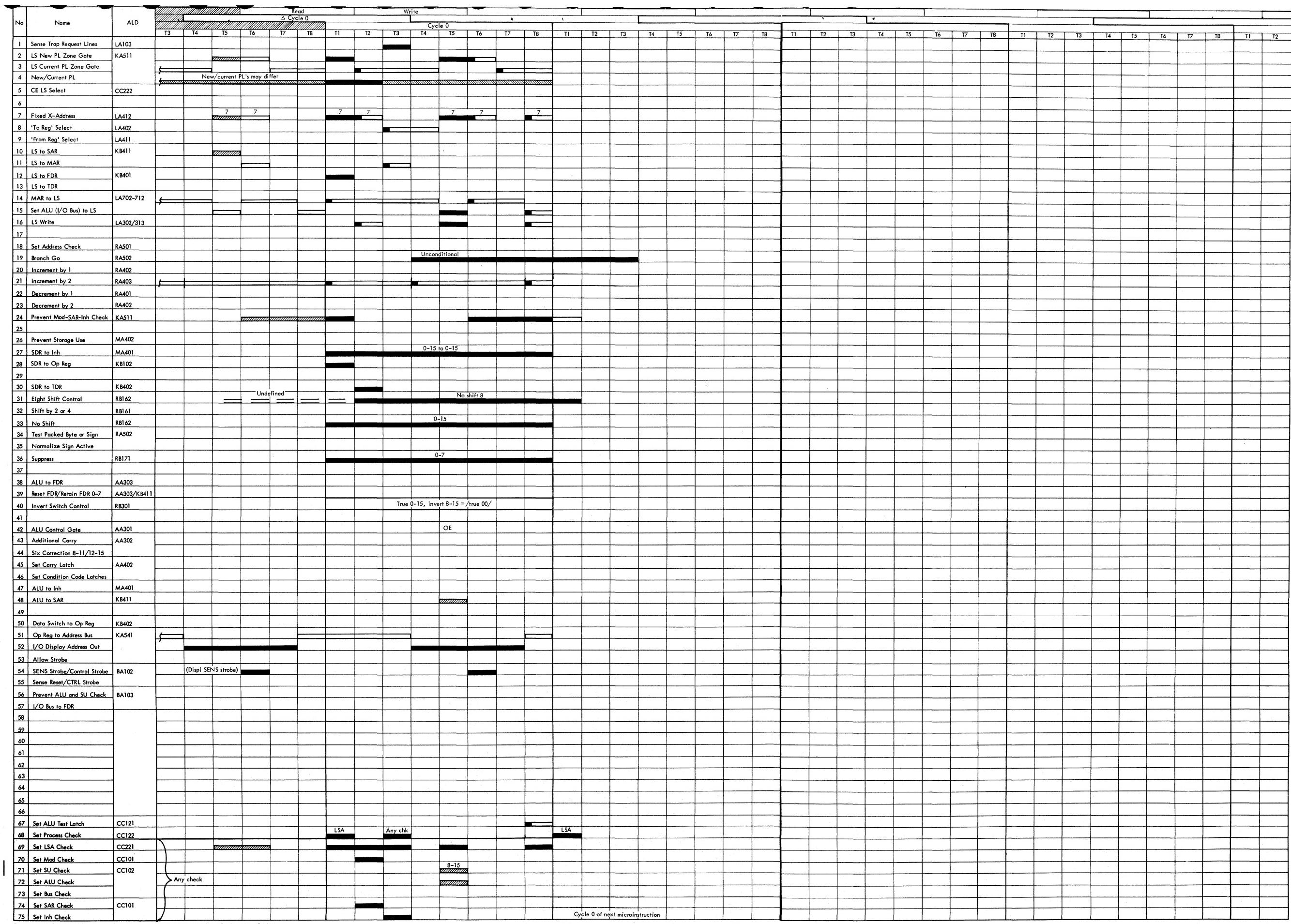
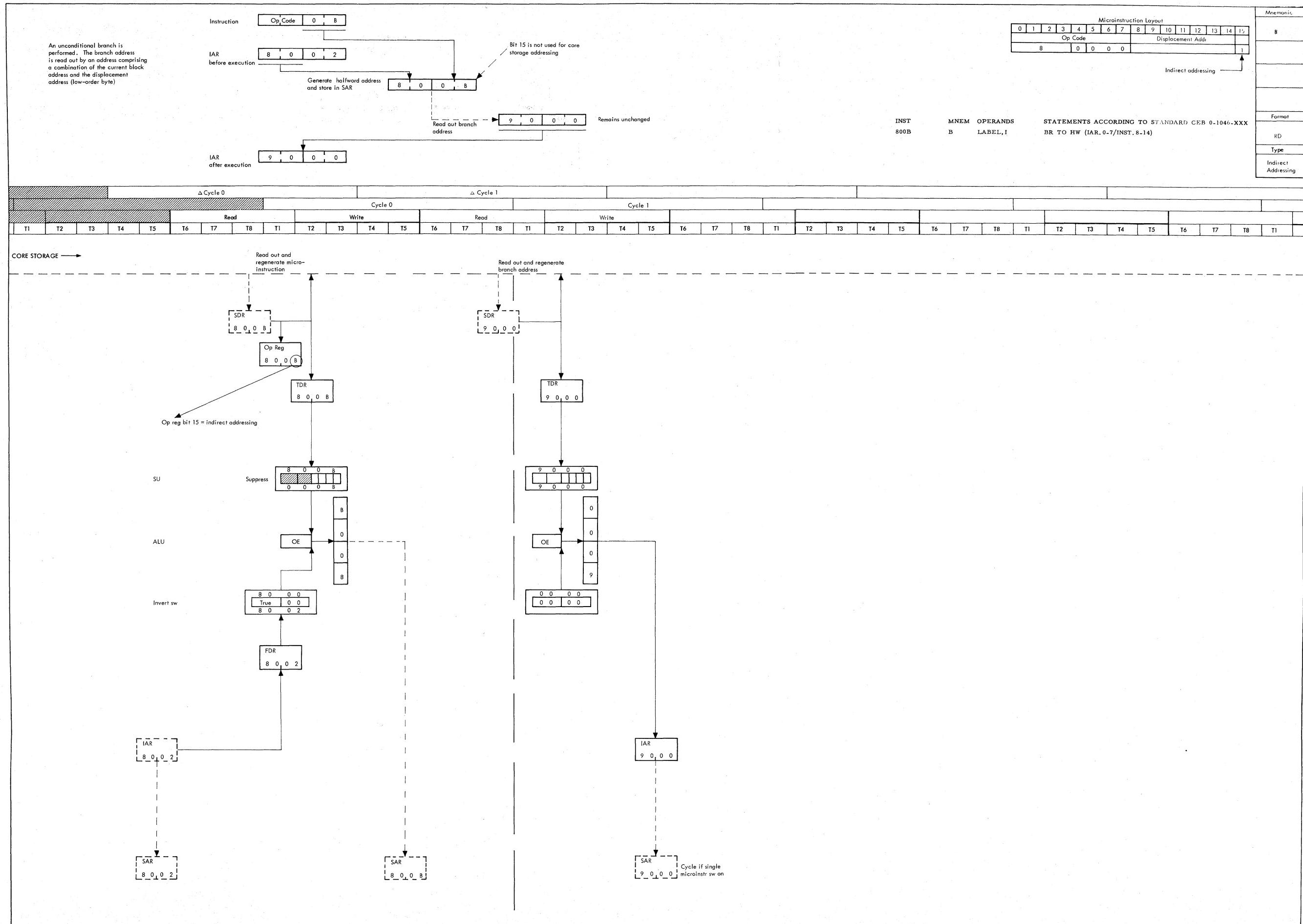


Diagram 5-20. Branch Unconditional (Direct Addressing) (Part 2 of 2) (03725A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

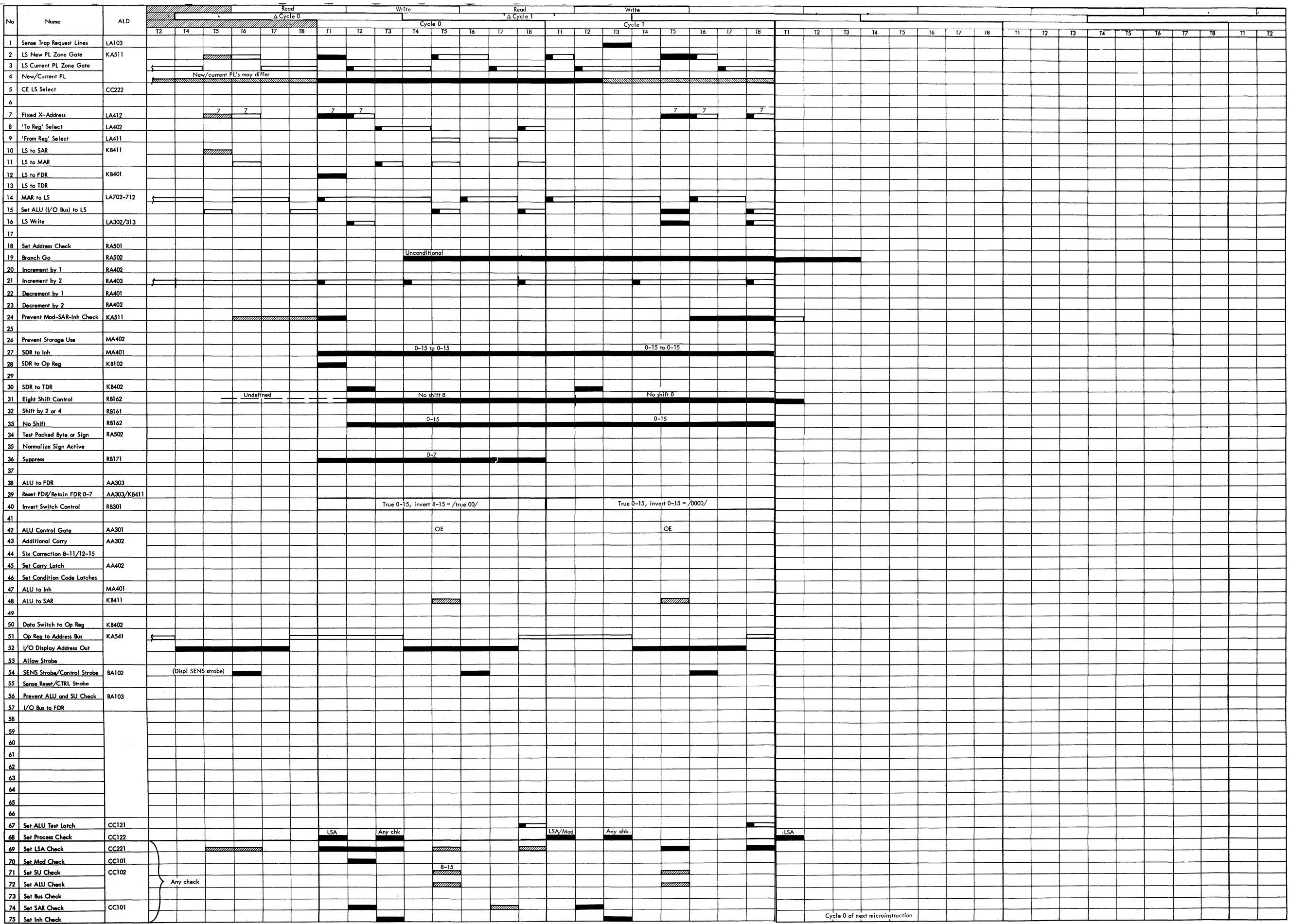


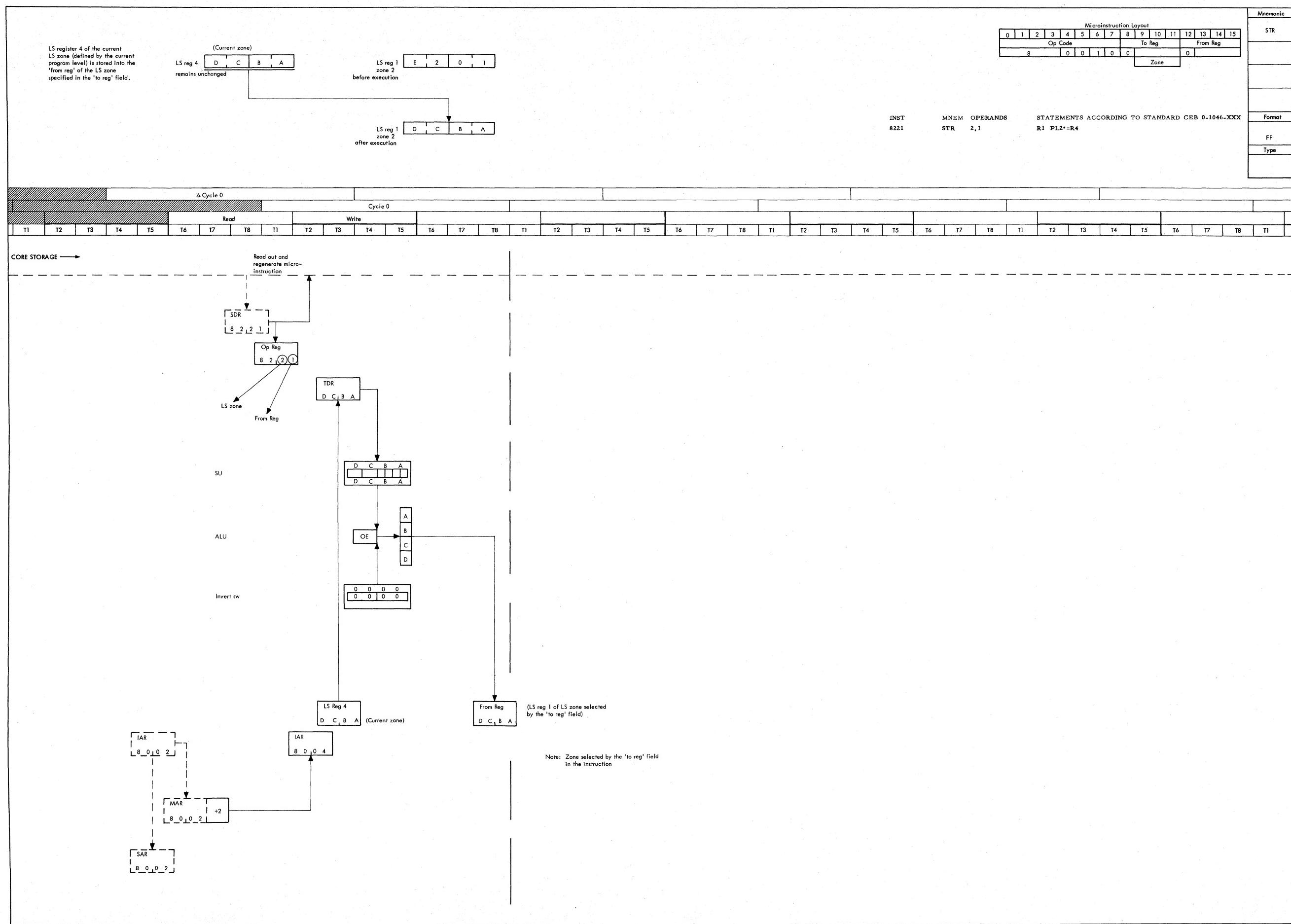
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:

- △Cycle
- Cycle



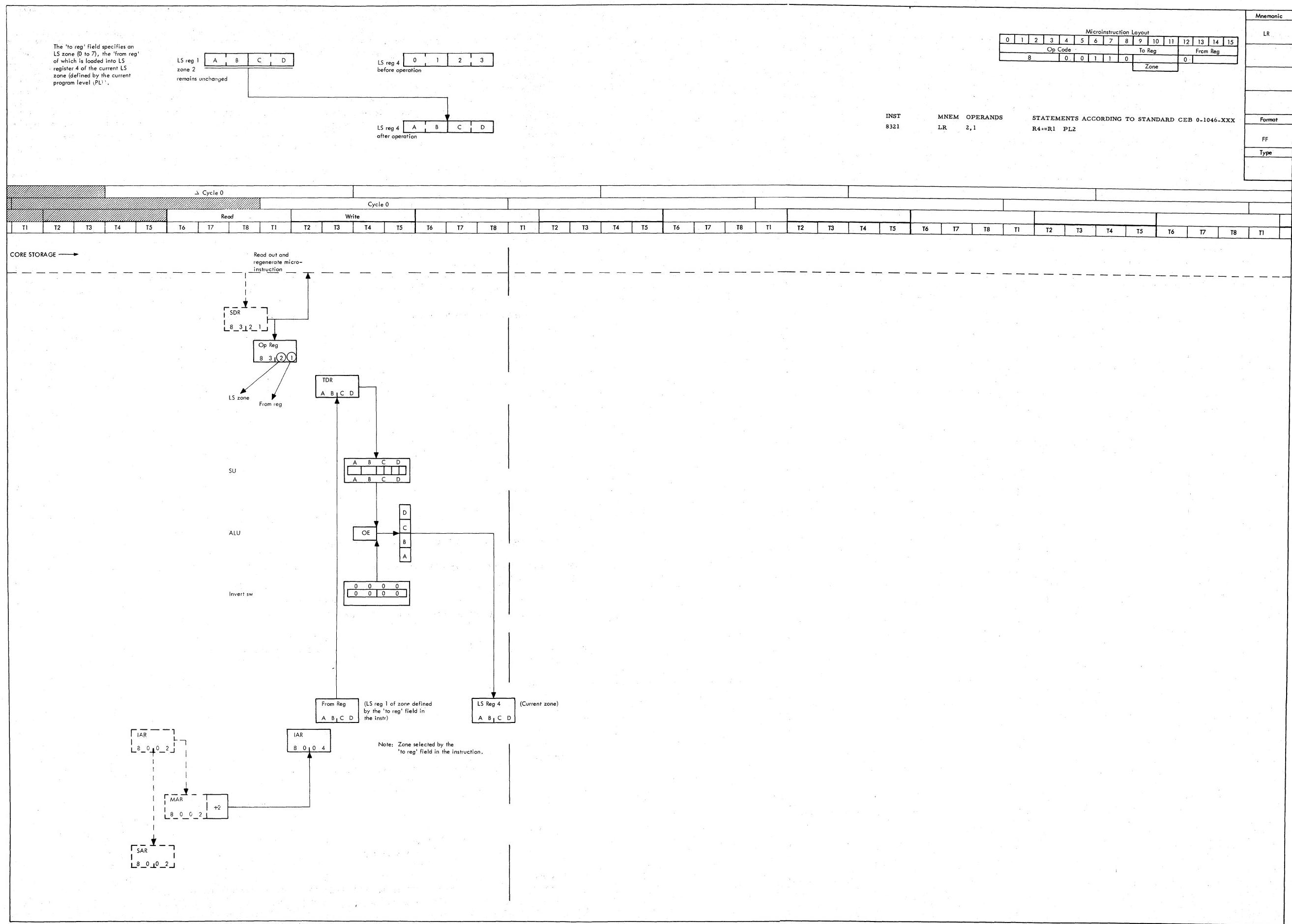


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

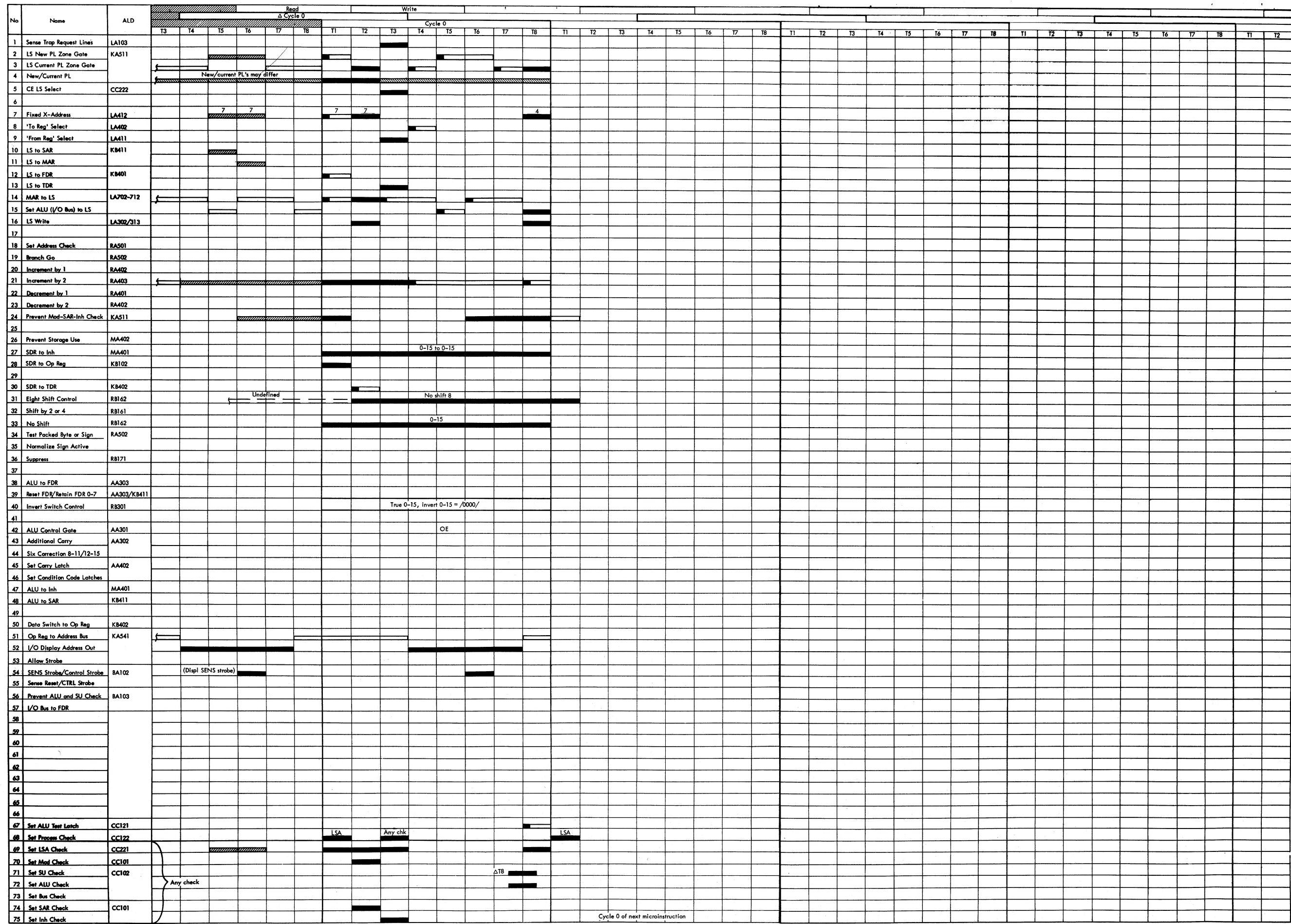
Diagram 5-22. Store Zone Register (Part 1 of 2) (03727) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

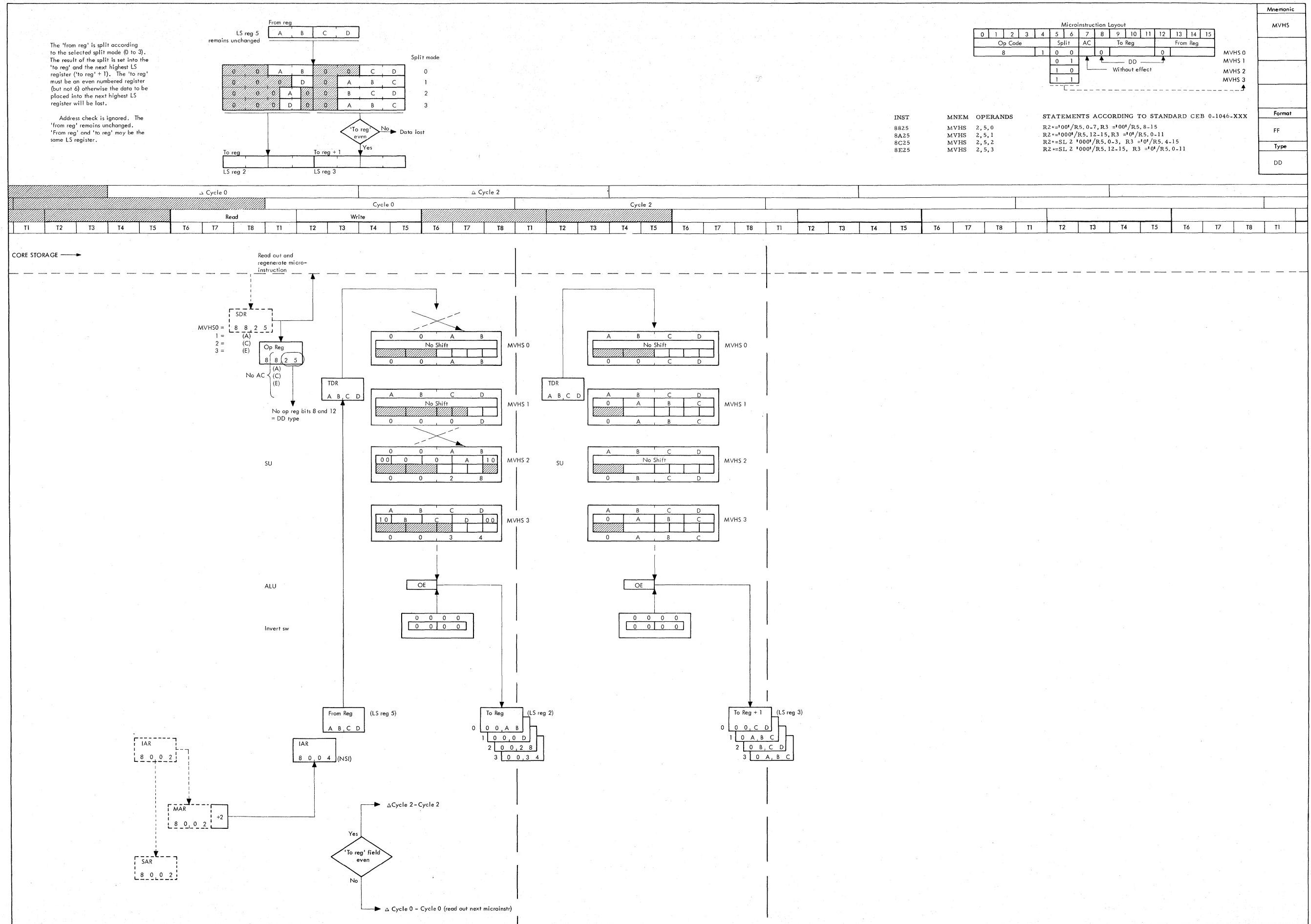
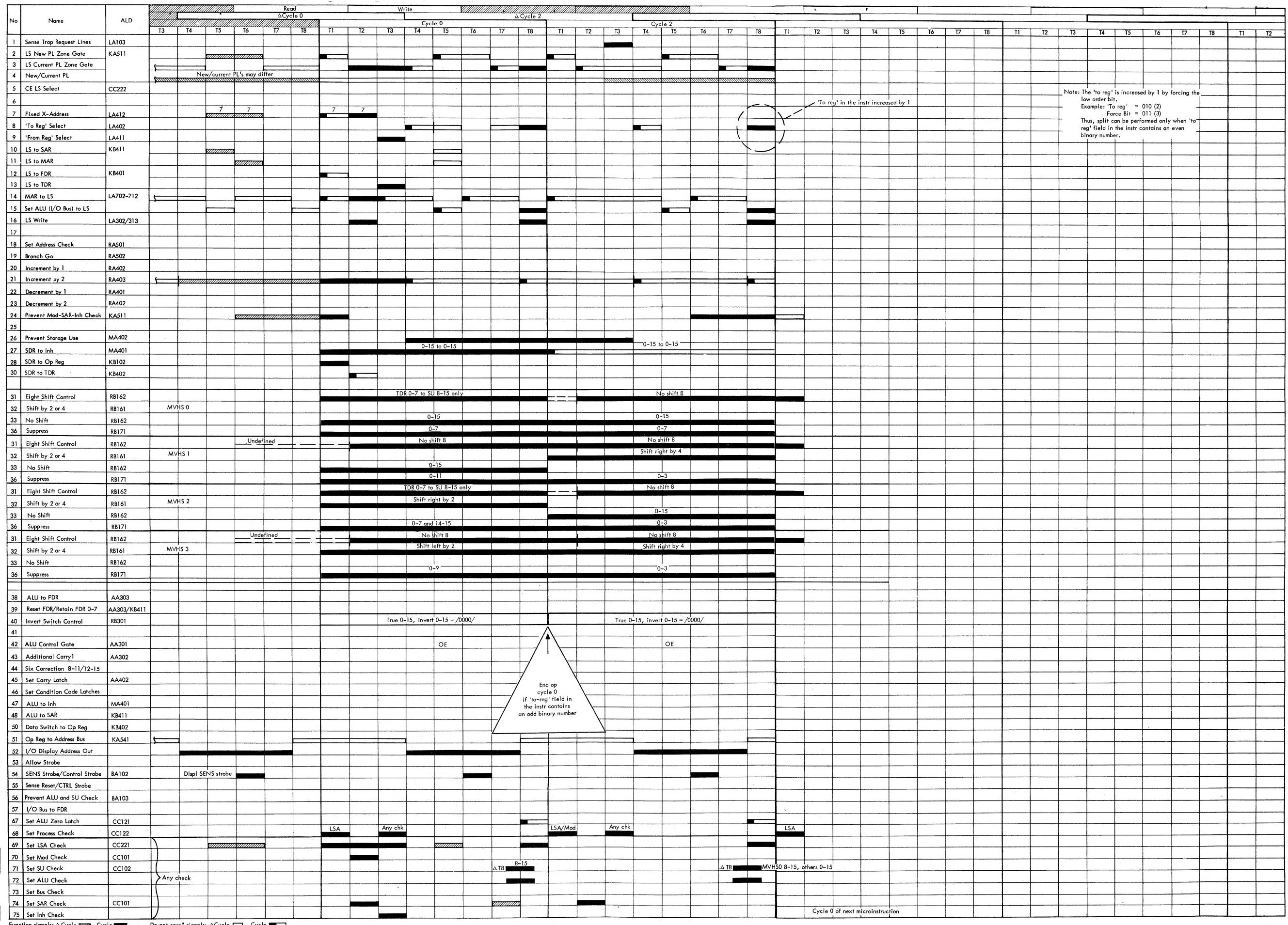
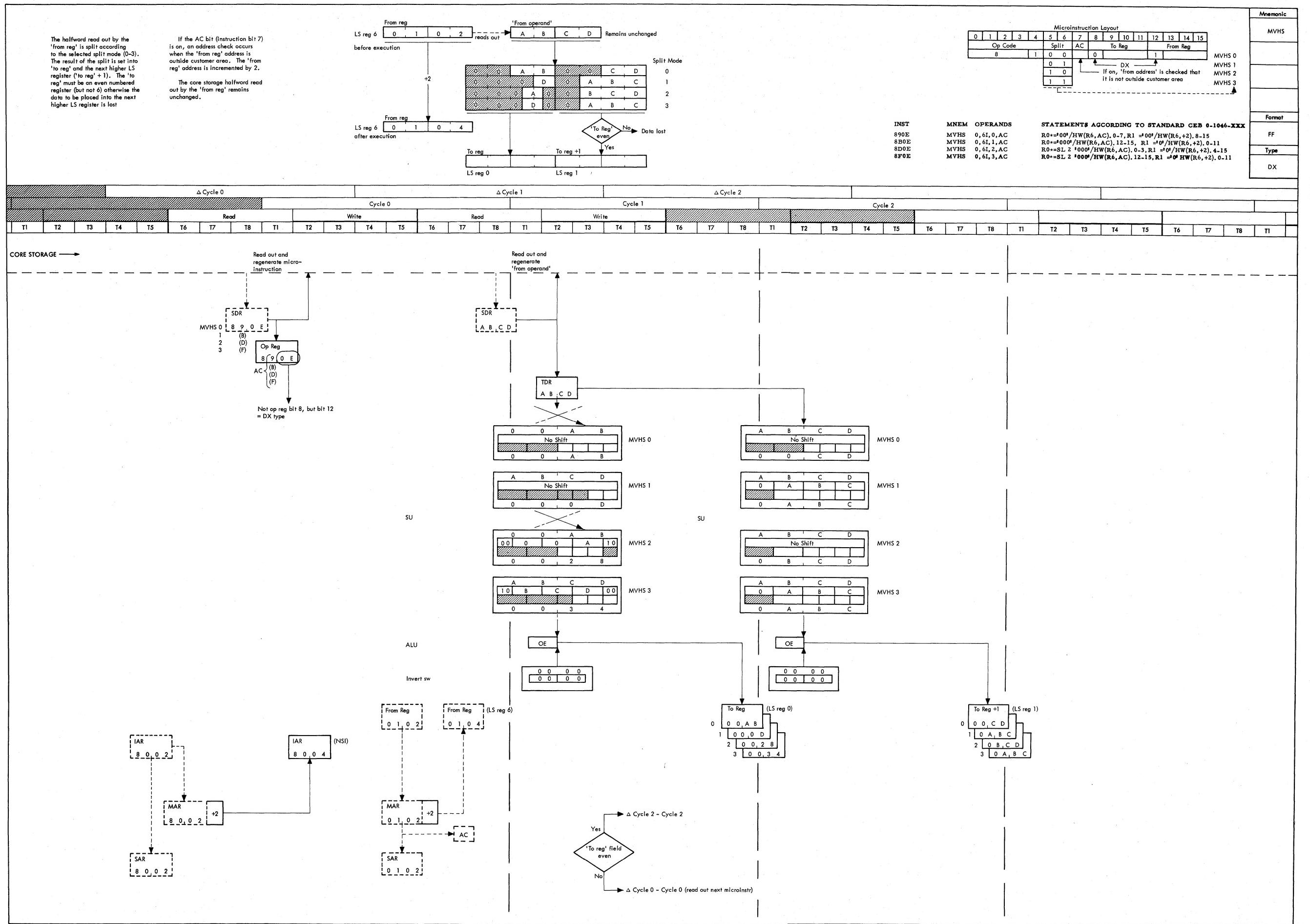
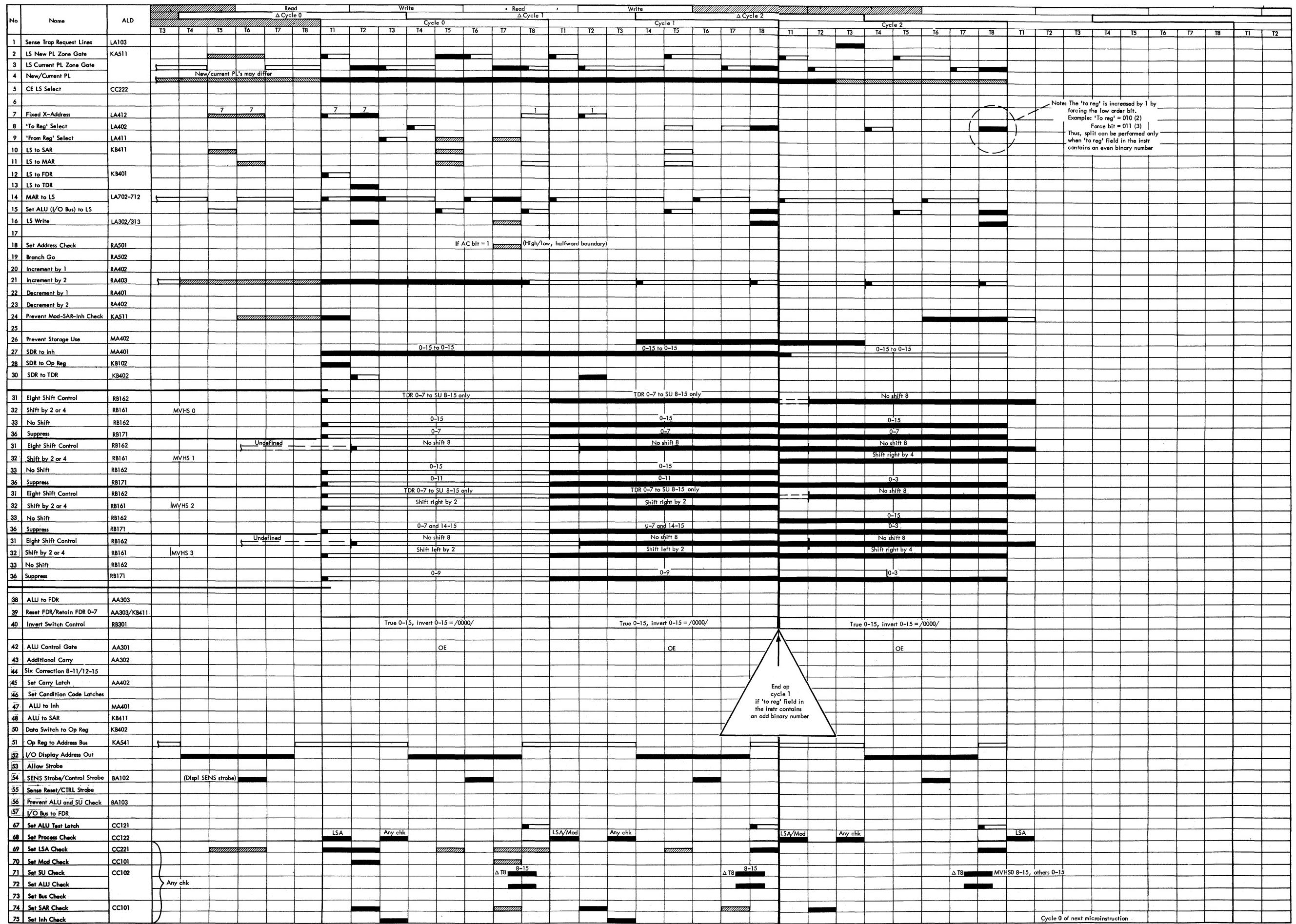


Diagram 5-24. Move Halfword and Split(DD) (Part 1 of 2) (03729) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)



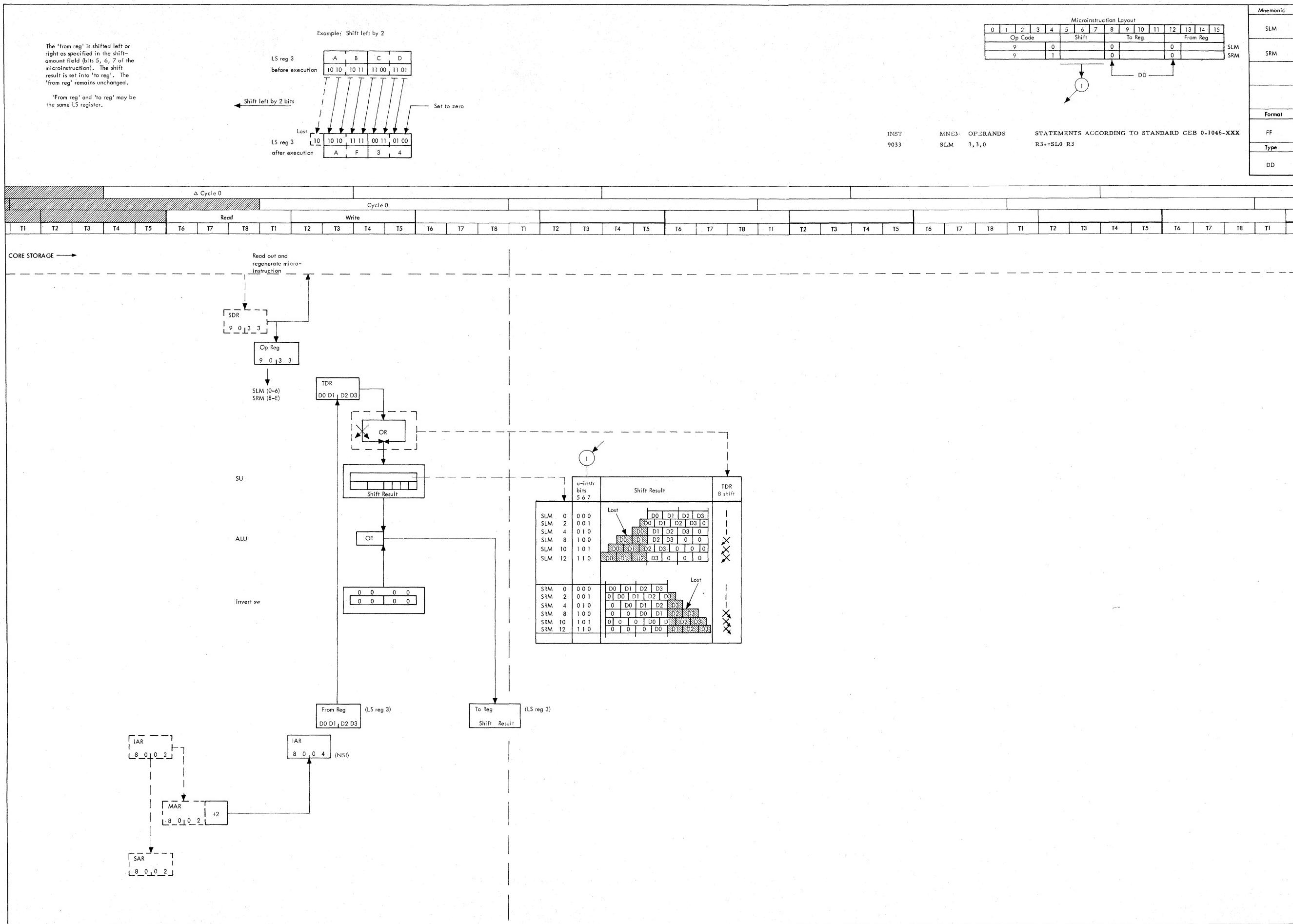
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle





Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

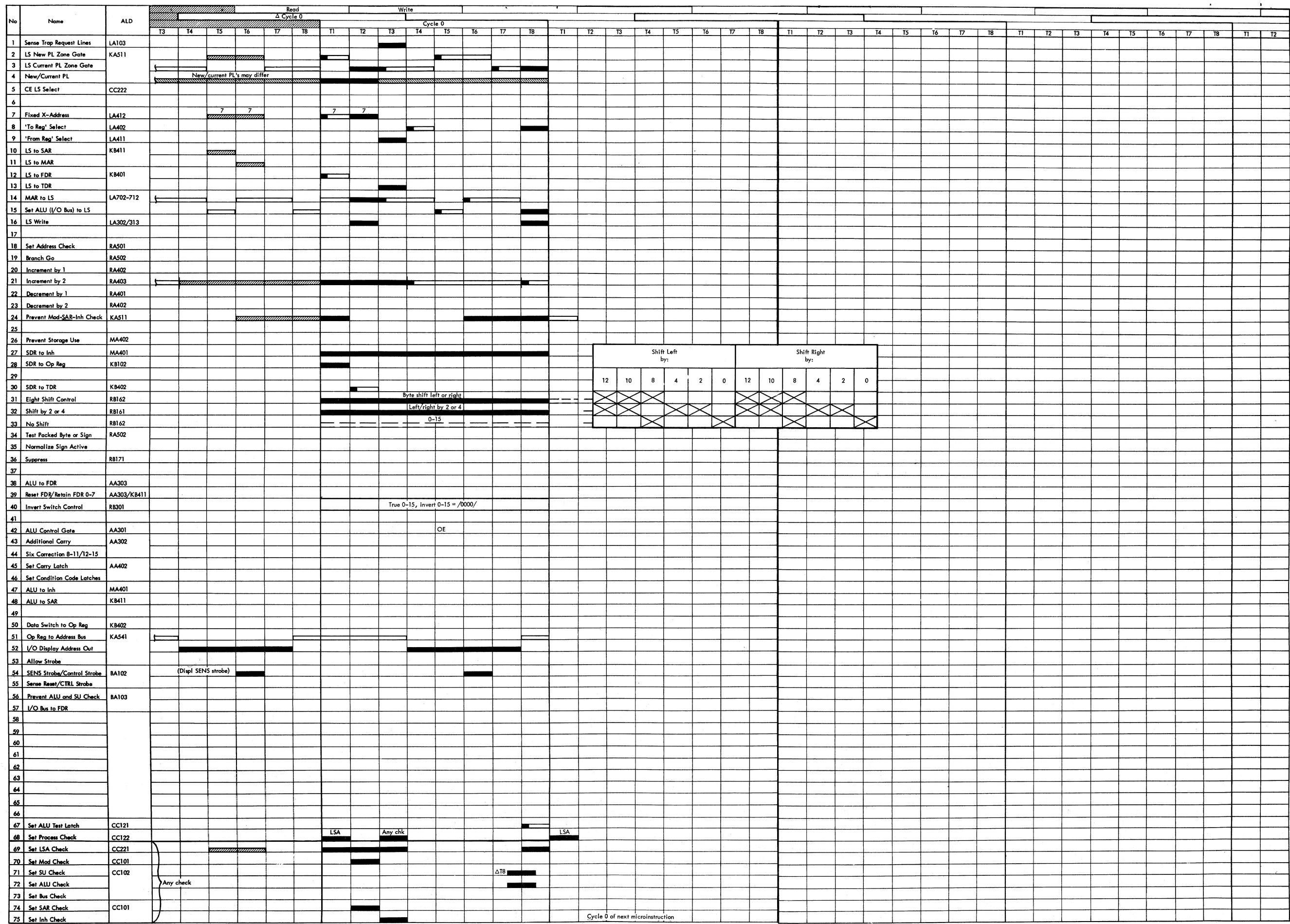
"Do not care" signals: Δ Cycle Cycle



Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:

Δ Cycle Cycle



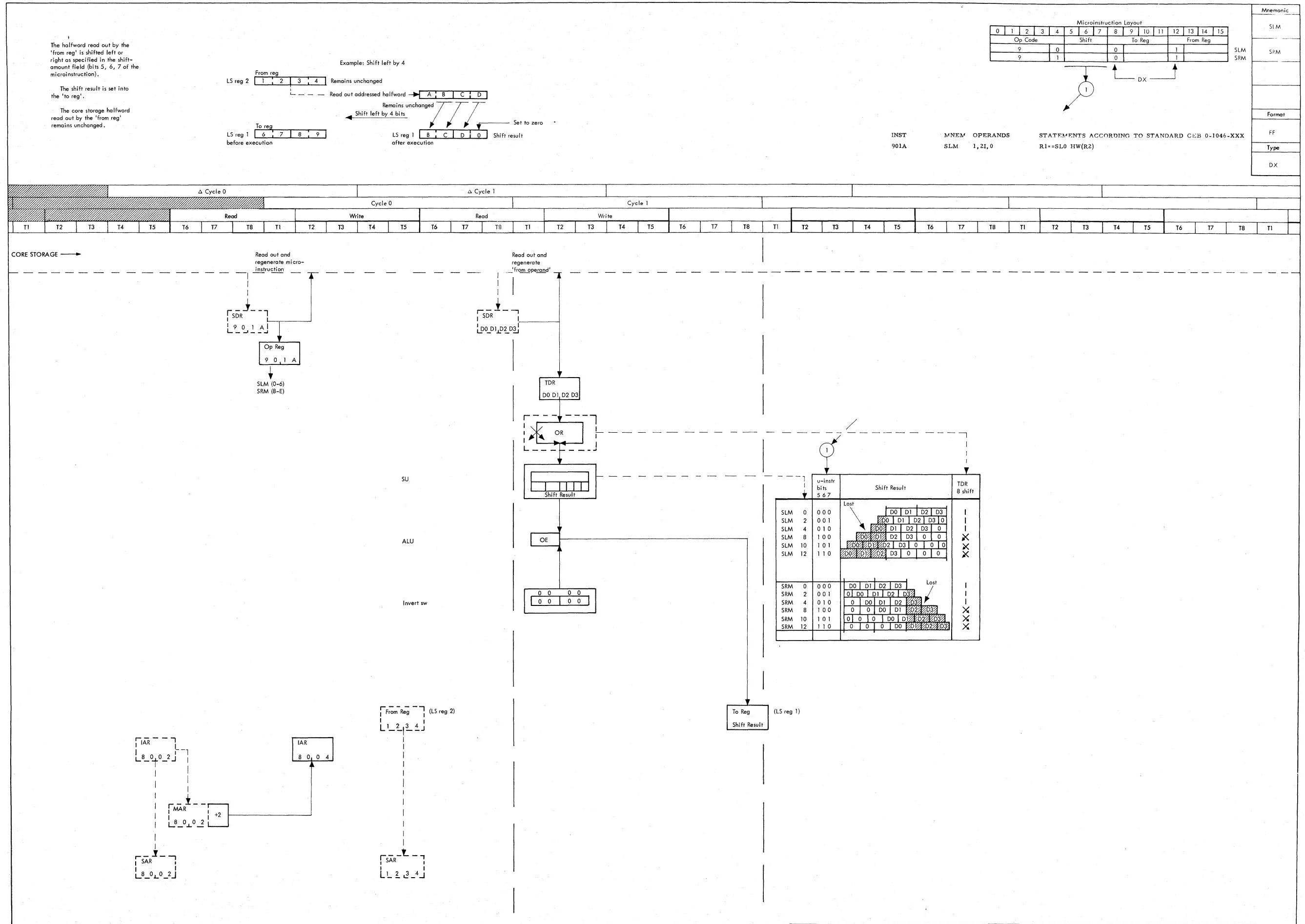
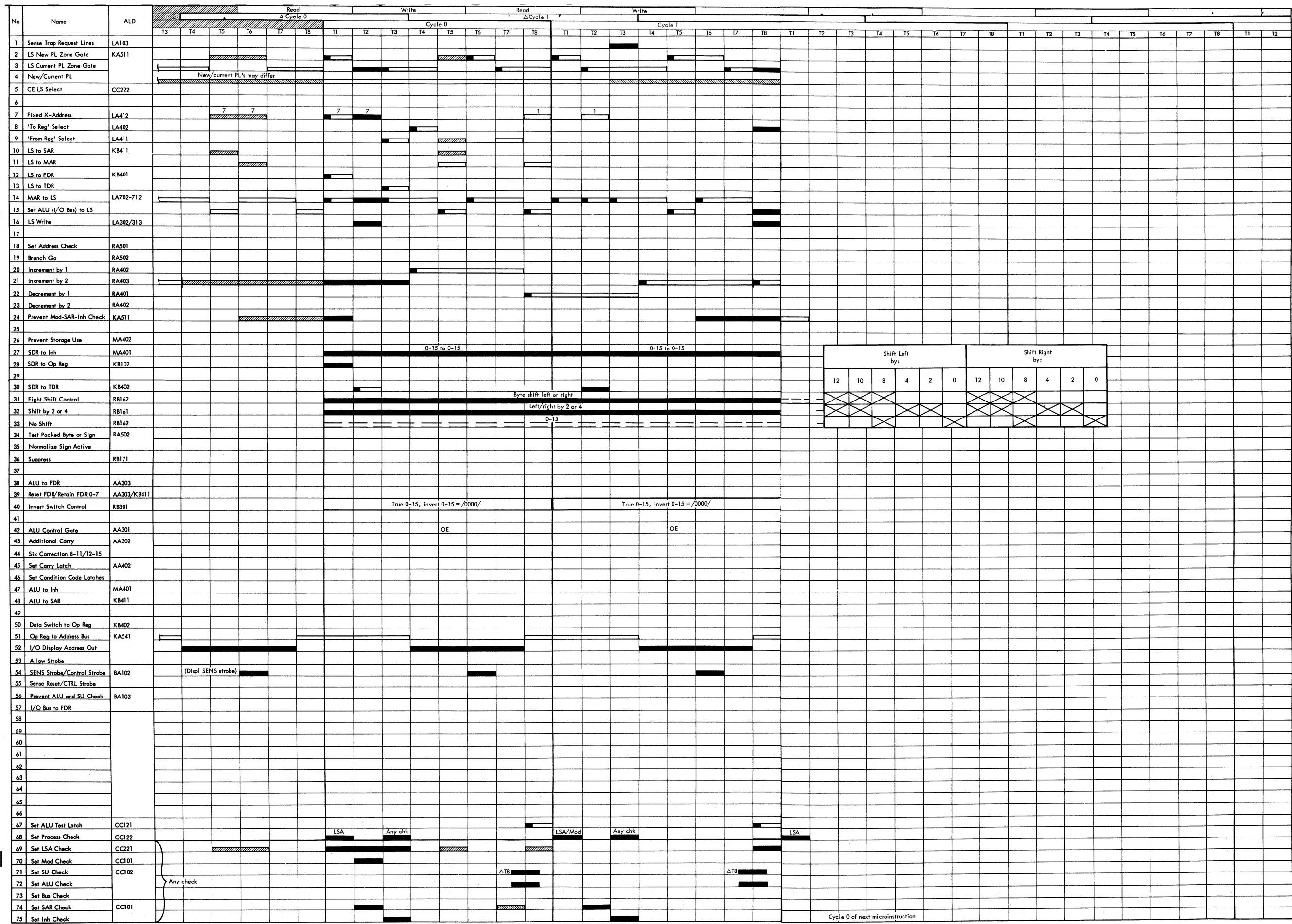
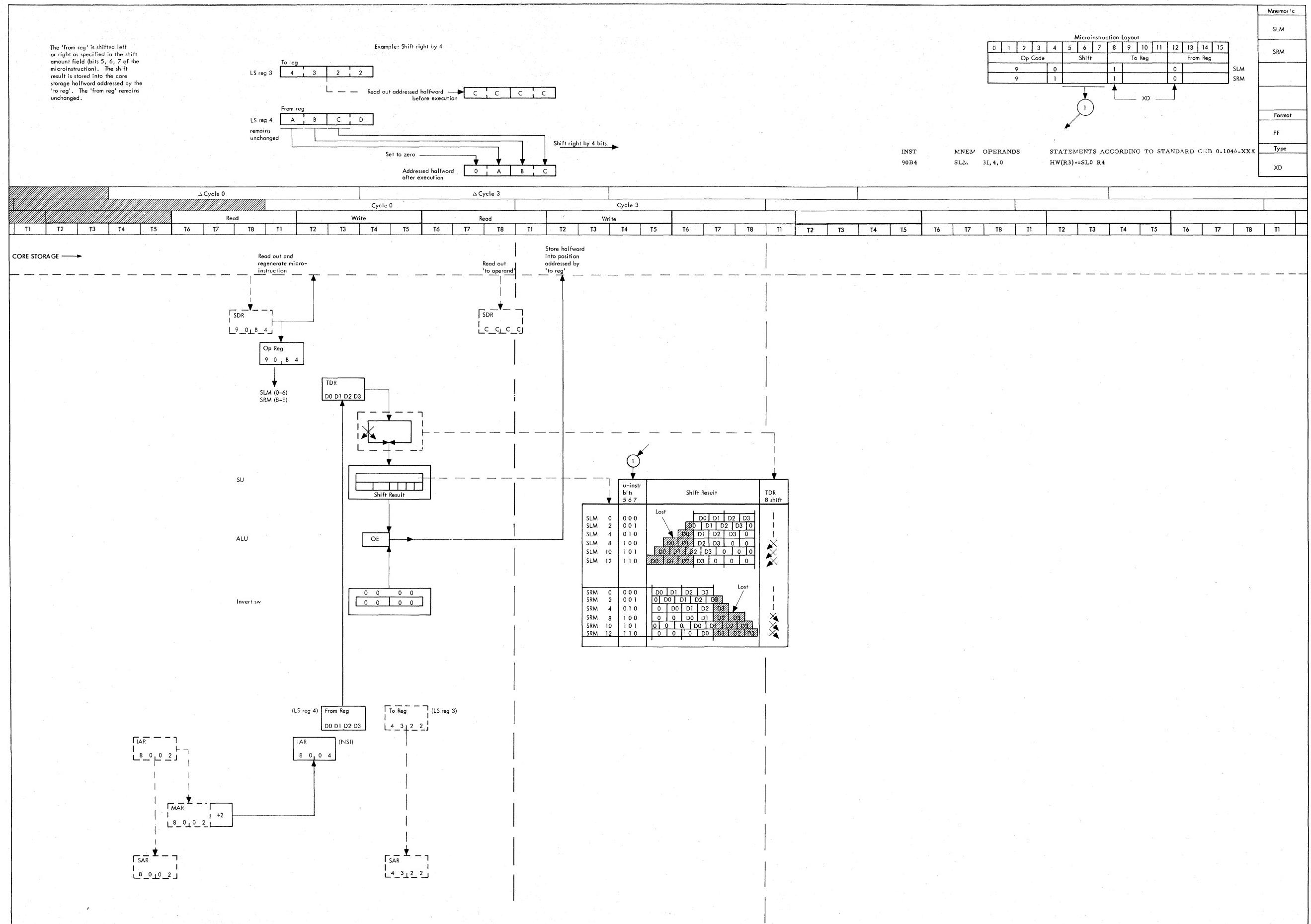


Diagram 5-27. Shift Left/Right and Move (DX) (Part 1 of 2) (03732) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

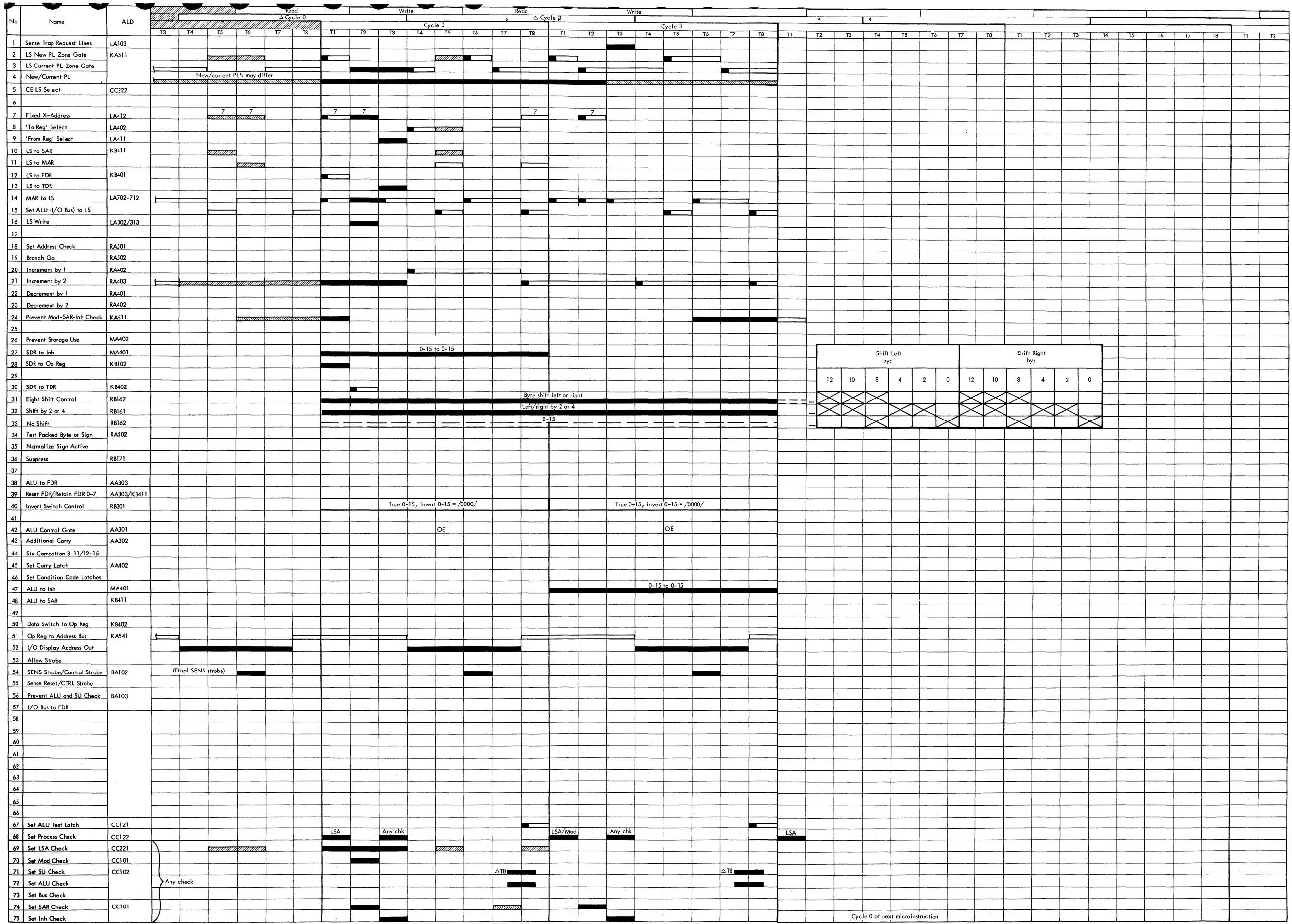
"Do not care" signals: Δ Cycle Cycle



Note: For "Do not care" functions refer to timing chart below.

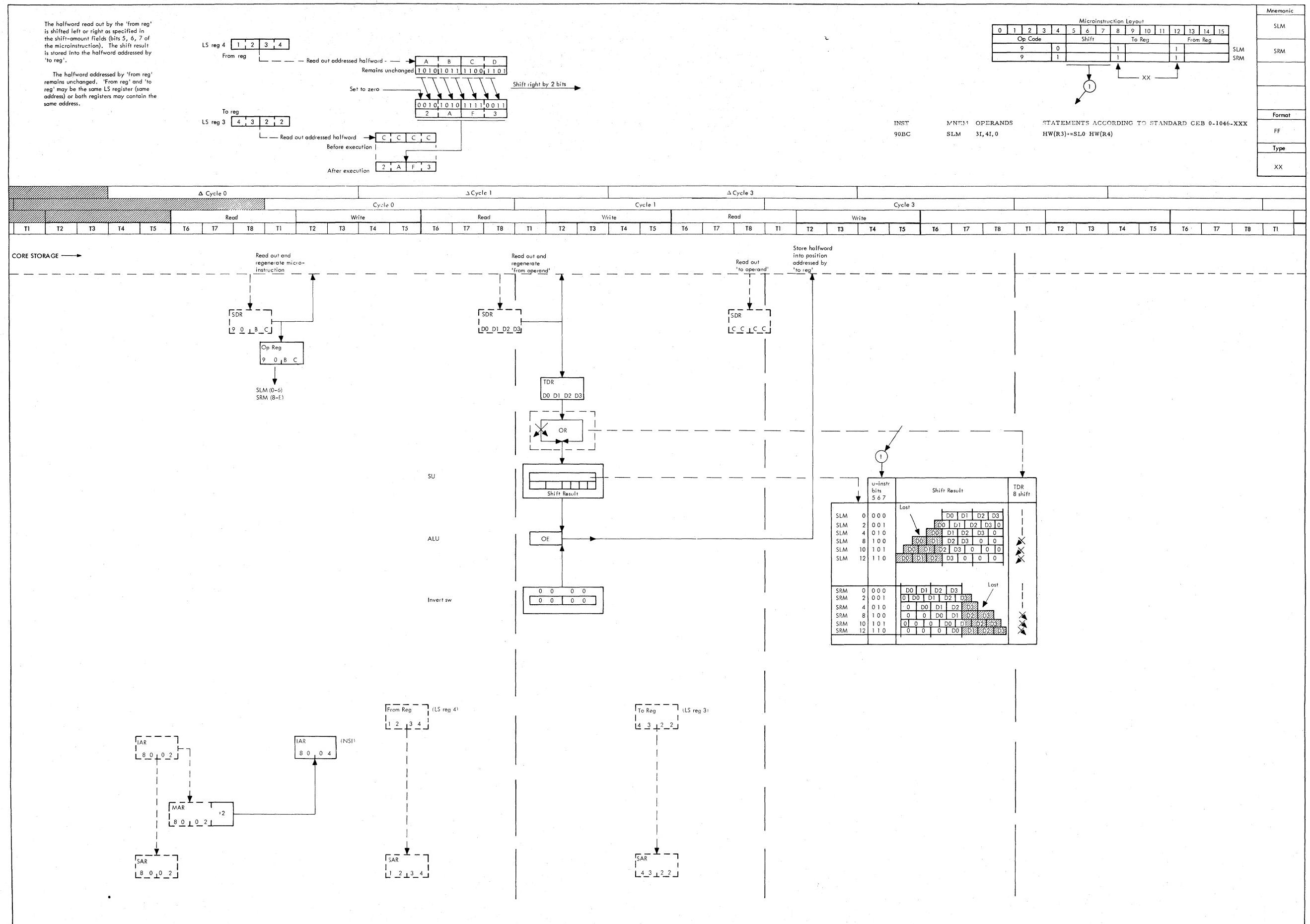
"Do not care" signals:
△Cycle **Cycle**

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: ΔCycle Cycle

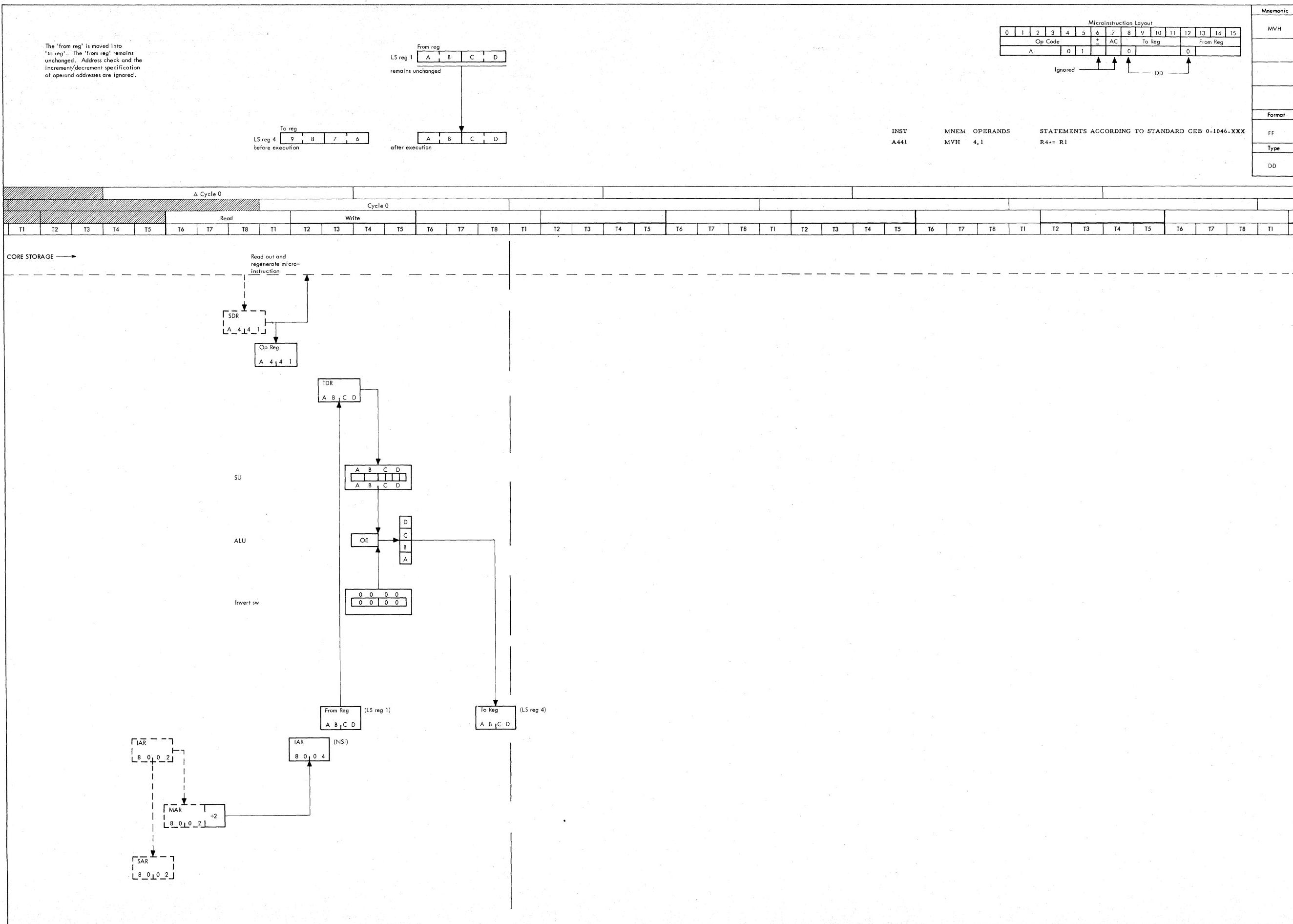


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD	Read								Write								Read								Write								Read									
			Δ Cycle 0				Cycle 0				Δ Cycle 1				Cycle 1				Δ Cycle 3				Cycle 3				Δ Cycle 4				Cycle 4				Δ Cycle 5				Cycle 5					
T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2					
1	Sense Trap Request Lines	LA103																																										
2	LS New PL Zone Gate	KA511																																										
3	LS Current PL Zone Gate																																											
4	New/Current PL																																											
5	CE LS Select	CC222																																										
6																																												
7	Fixed X-Address	LA	412	7	7			7	7								1	1									7	7																
8	'To Reg' Select	LA402																																										
9	'From Reg' Select	LA411																																										
10	LS to SAR	KB411																																										
11	LS to MAR																																											
12	LS to FDR	KB401																																										
13	LS to TDR																																											
14	MAR to LS	LA702-712																																										
15	Set ALU (I/O Bus) to LS																																											
16	LS Write	LA302/313																																										
17																																												
18	Set Address Check	RA501																																										
19	Branch Go	RA502																																										
20	Increment by 1	RA402																																										
21	Increment by 2	RA403																																										
22	Decrement by 1	RA401																																										
23	Decrement by 2	RA402																																										
24	Prevent Mod-SAR-Inh Check	KA511																																										
25																																												
26	Prevent Storage Use	MA402																																										
27	SDR to Inh	MA401																																										
28	SDR to Op Reg	KB102																																										
29																																												
30	SDR to TDR	KB402																																										
31	Eight Shift Control	RB162																																										
32	Shift by 2 or 4	RB161																																										
33	No Shift	RB162																																										
34	Test Packed Byte or Sign	RA502																																										
35	Normalize Sign Active																																											
36	Suppress	RB171																																										
37																																												
38	ALU to FDR	AA303																																										
39	Reset FDR/Retain FDR 0-7	AA303/KB41																																										

Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

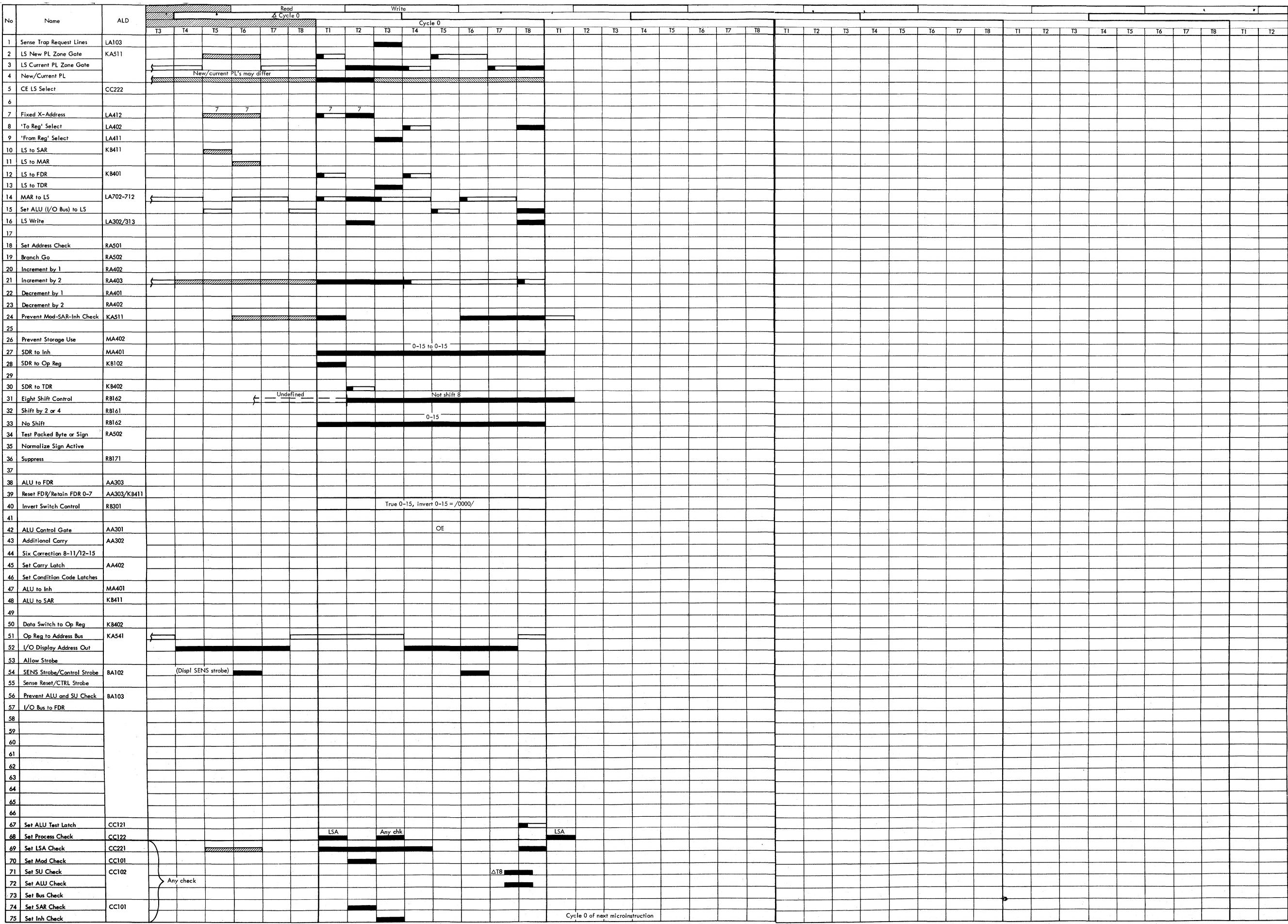
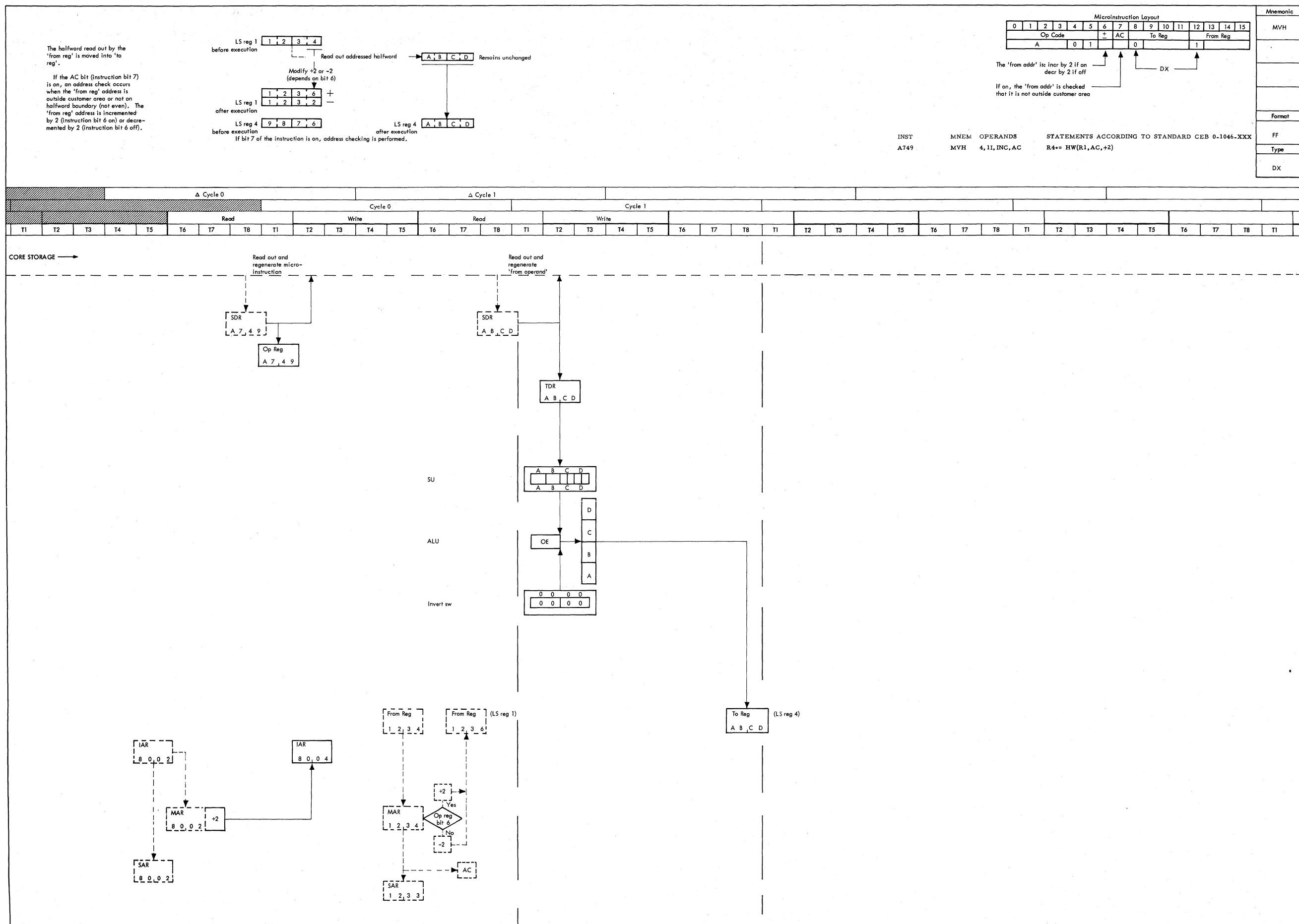
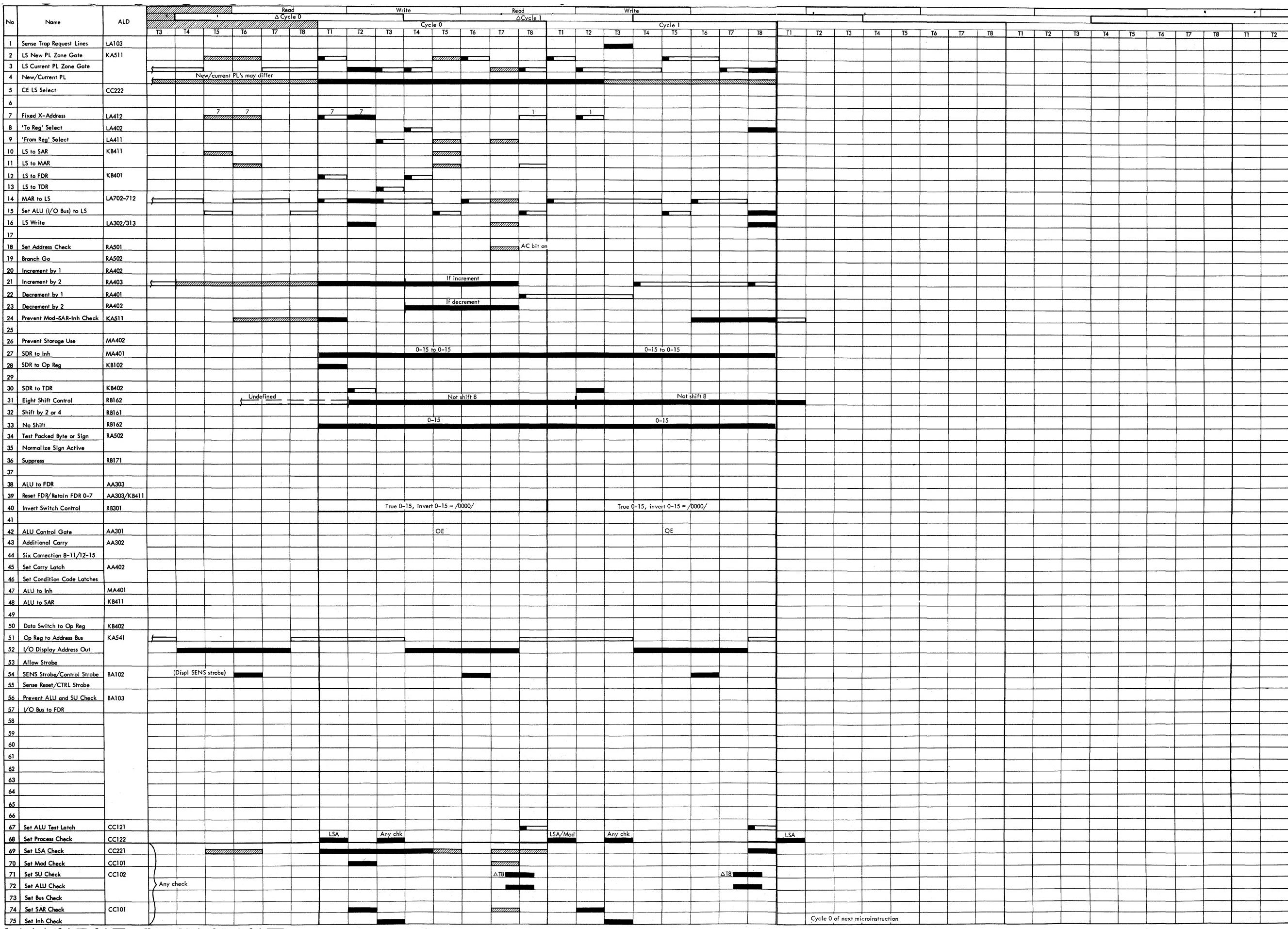
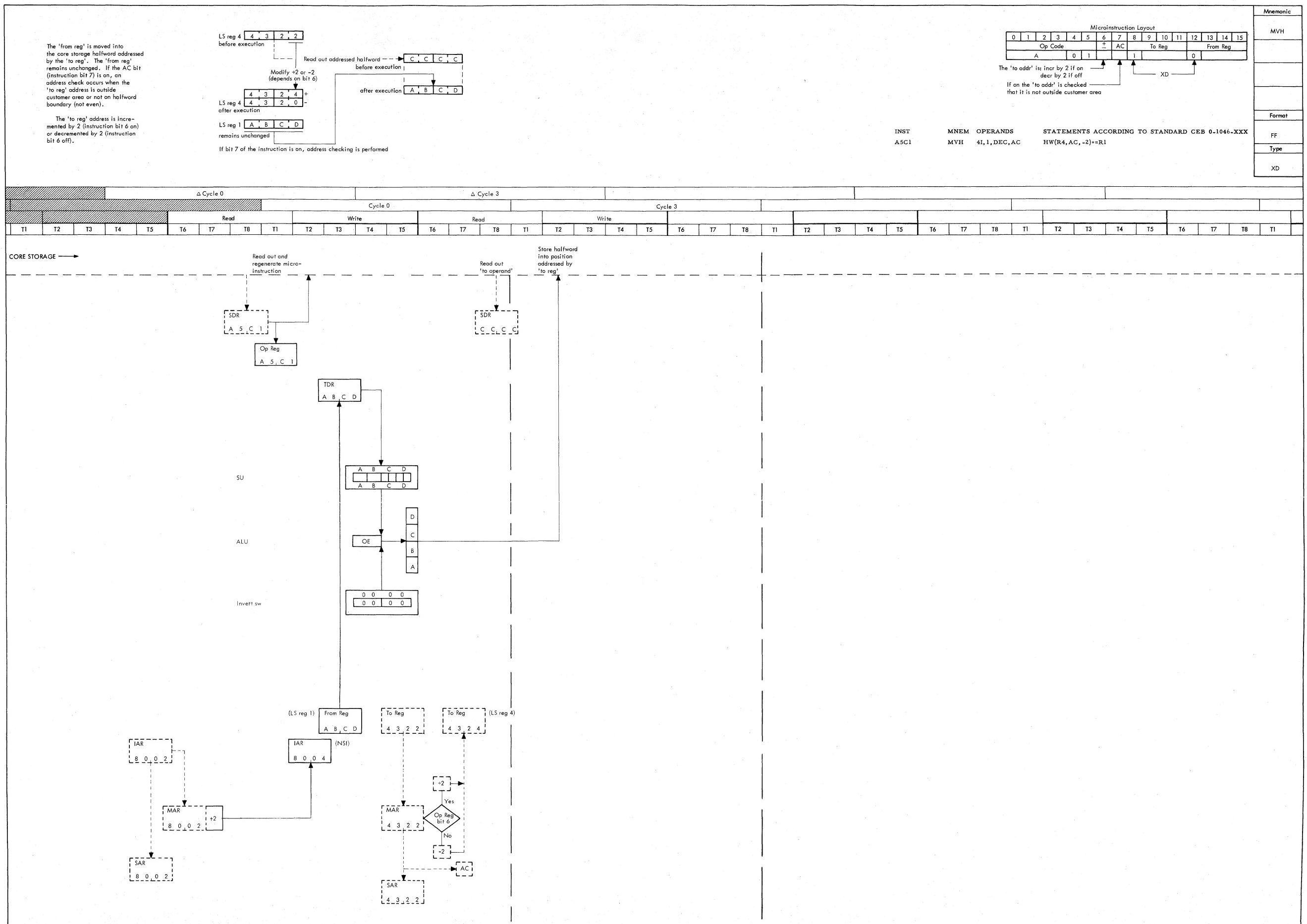


Diagram 5-30. Move Halfword (DD) (Part 2 of 2) (03735A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

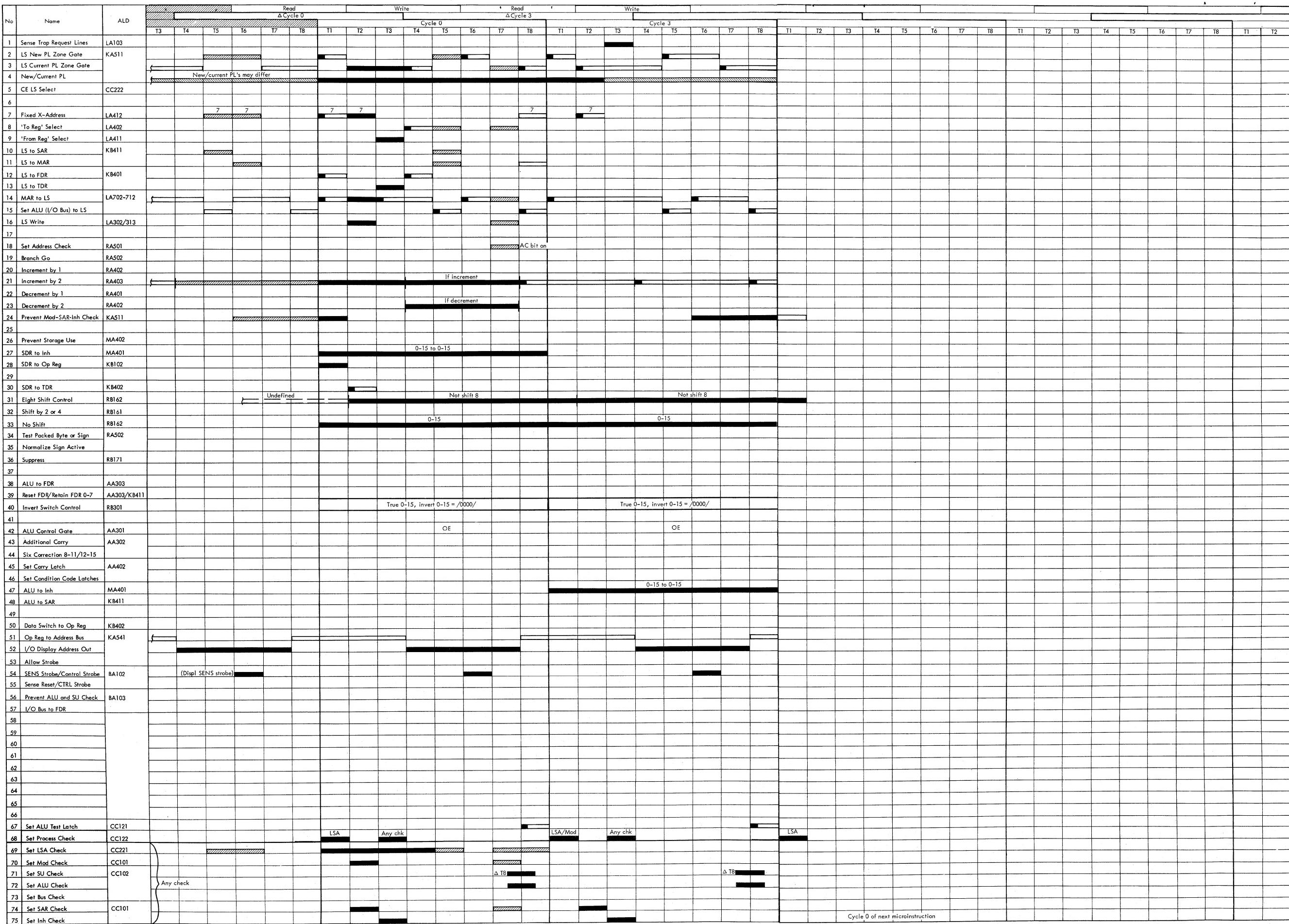


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



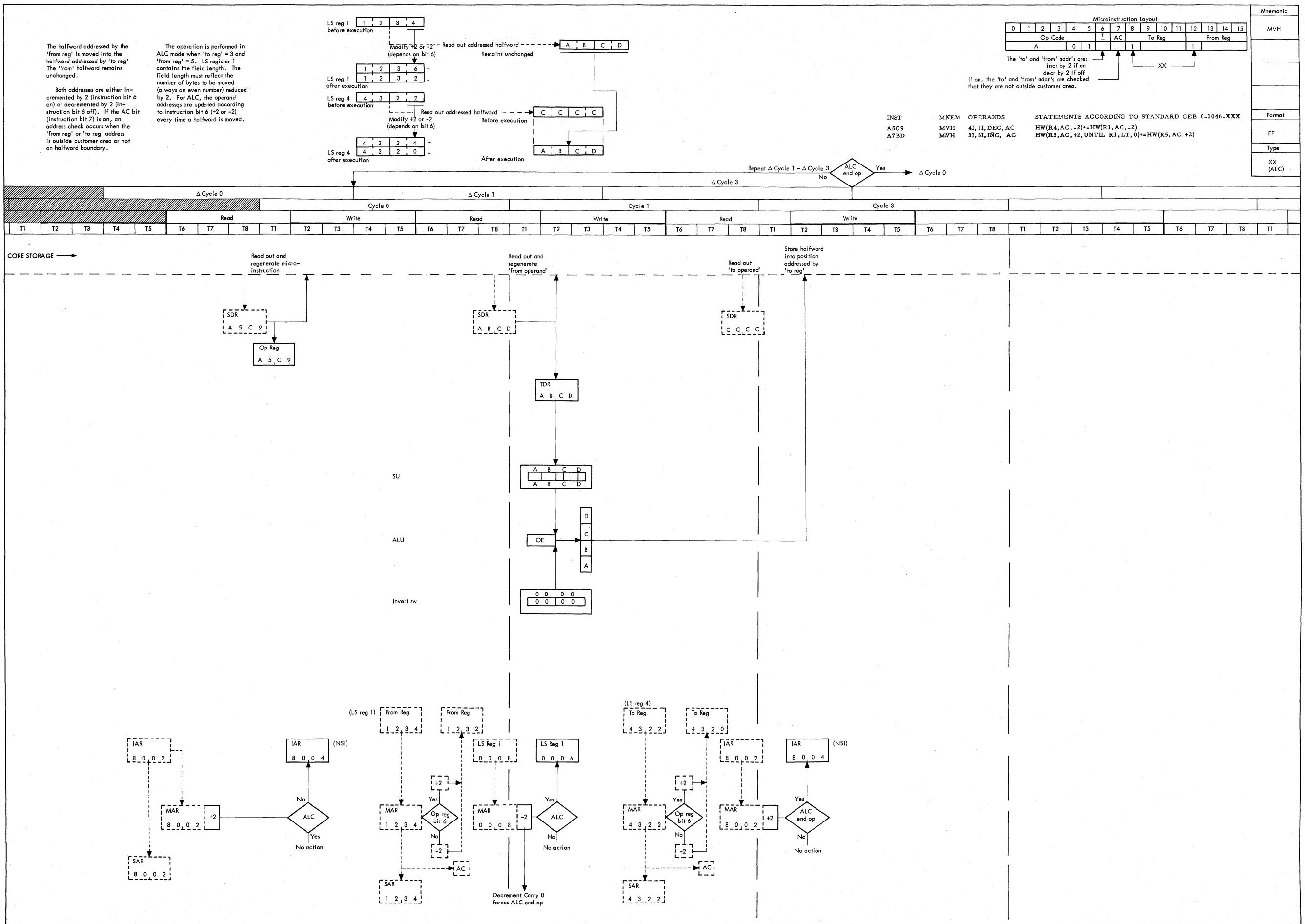


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



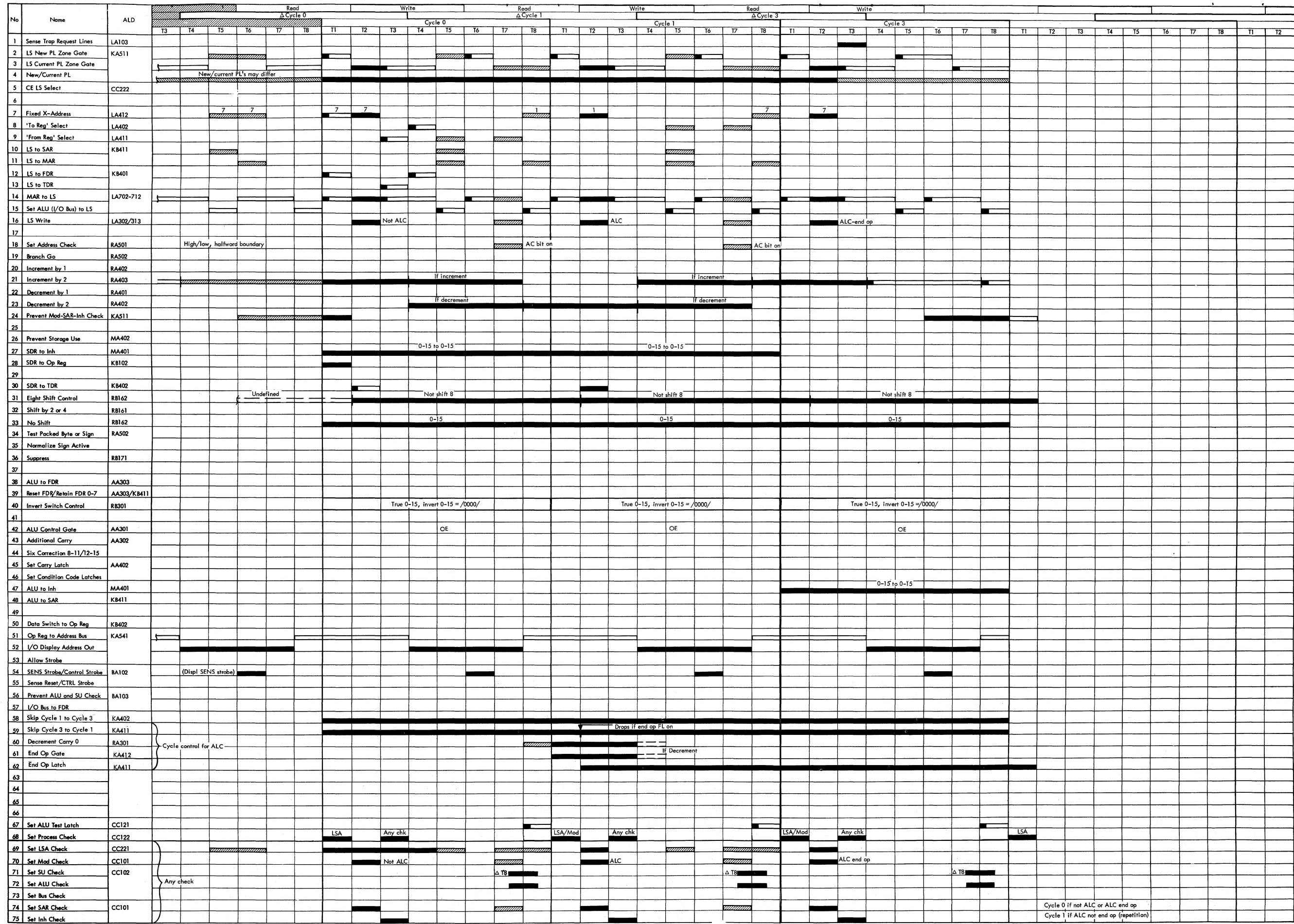
Function signals: ΔCycle Cycle

"Do not care" signals: ΔCycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

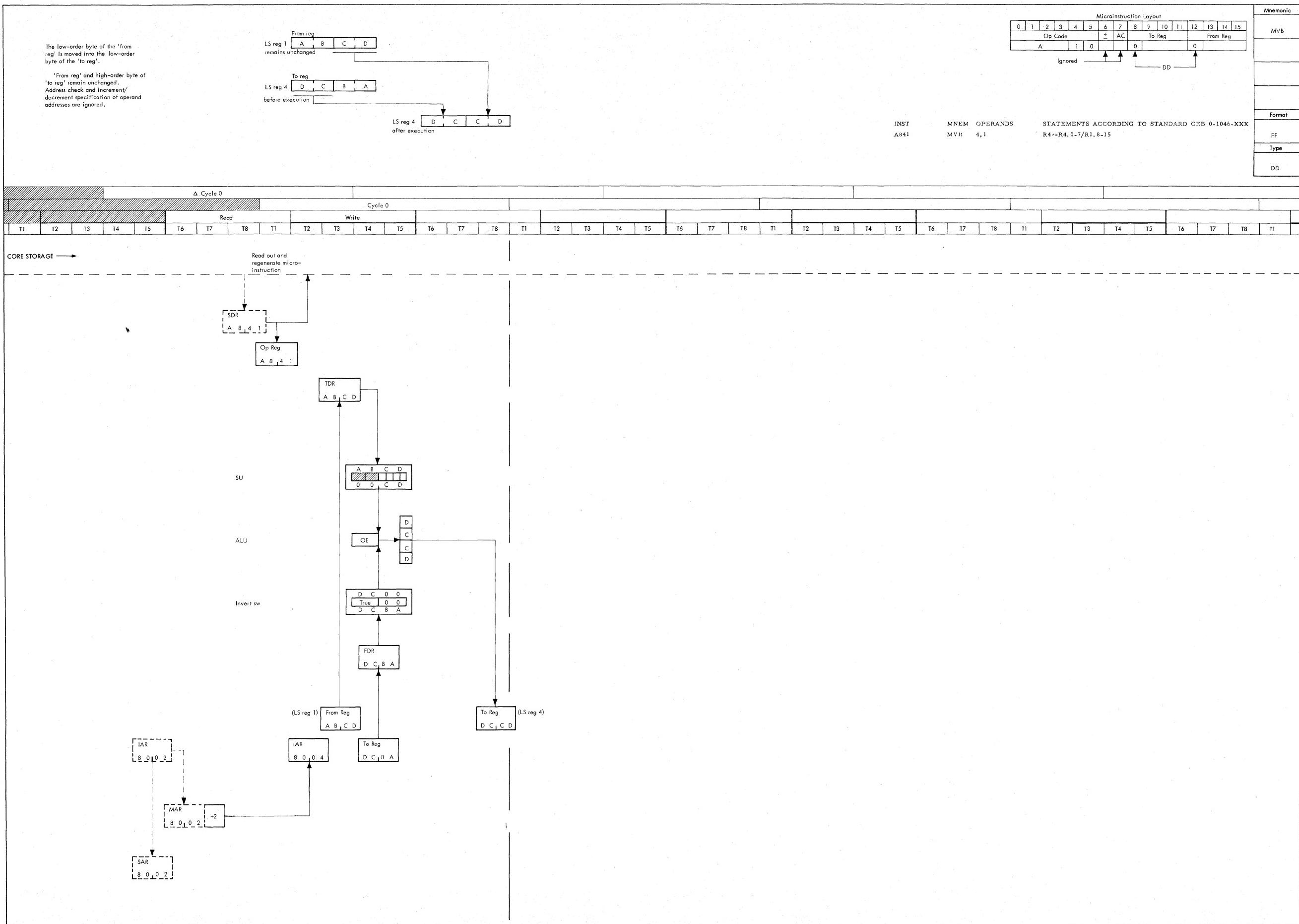
Diagram 5-33. Move Halfword (XX, ALC) (Part 1 of 2) (03738A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

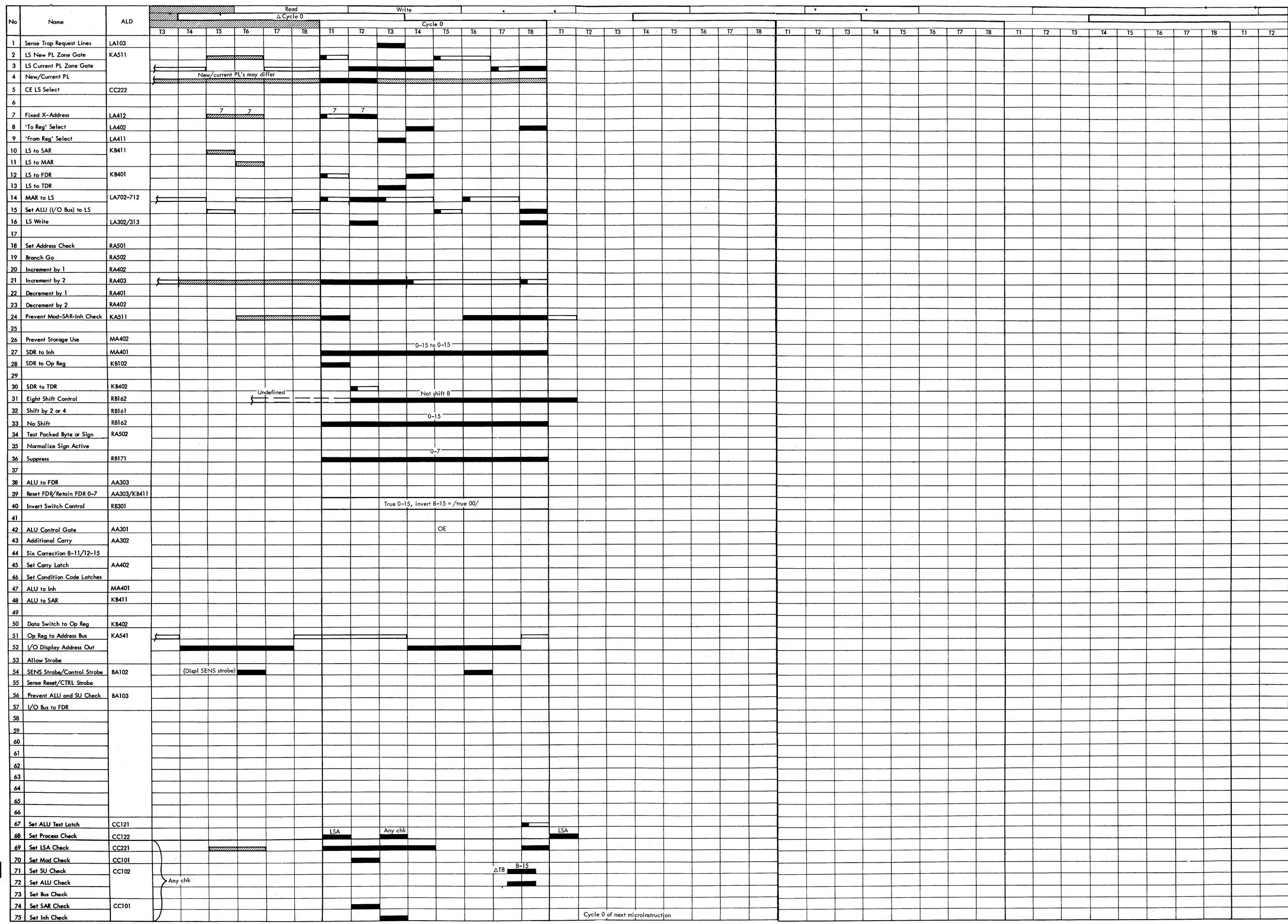
10. The following table shows the number of hours worked by each employee.



Note: For "Do not care" functions refer to timing chart below.

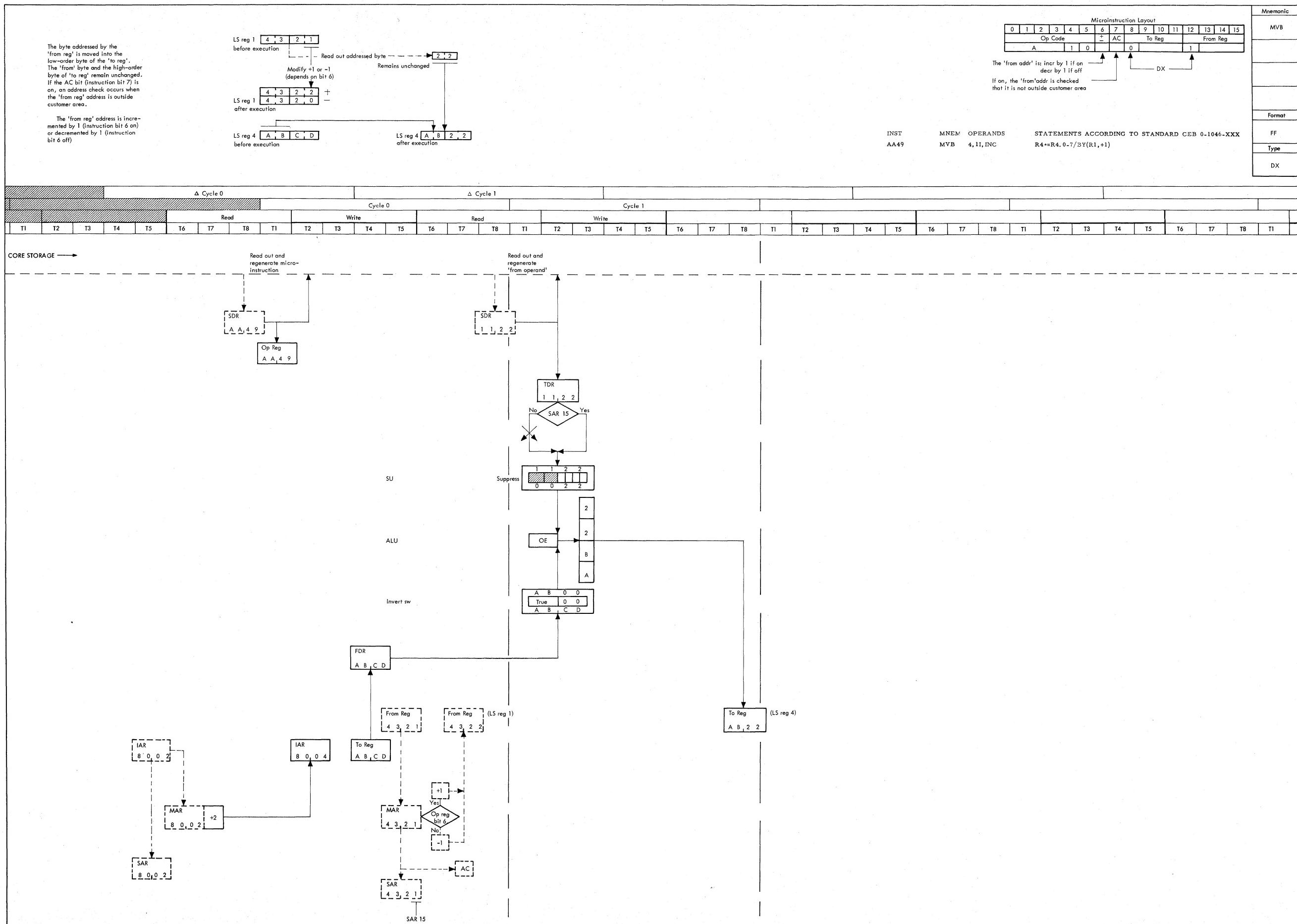
"Do not care" signals:
 ΔCycle:
 Cycle:

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

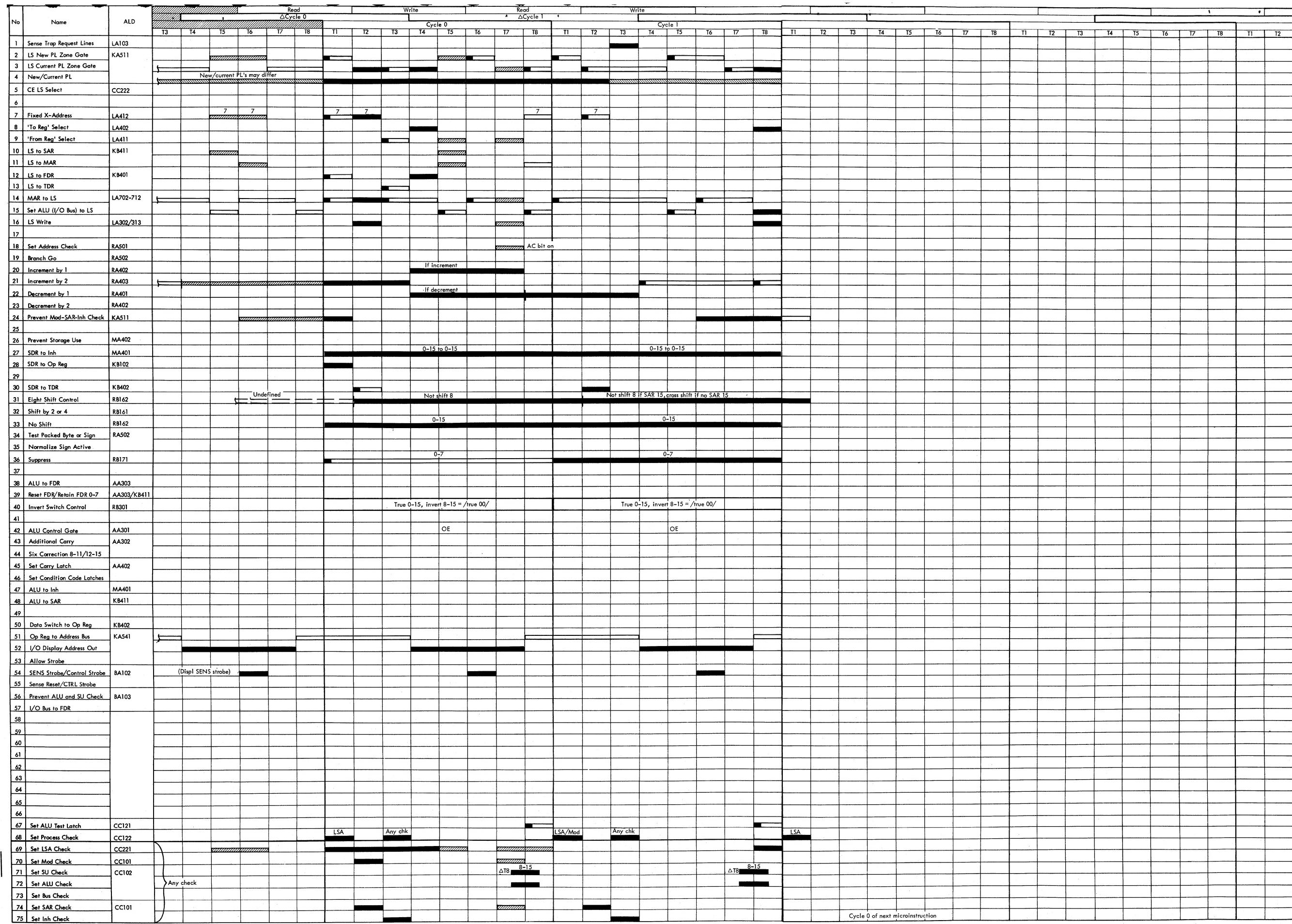


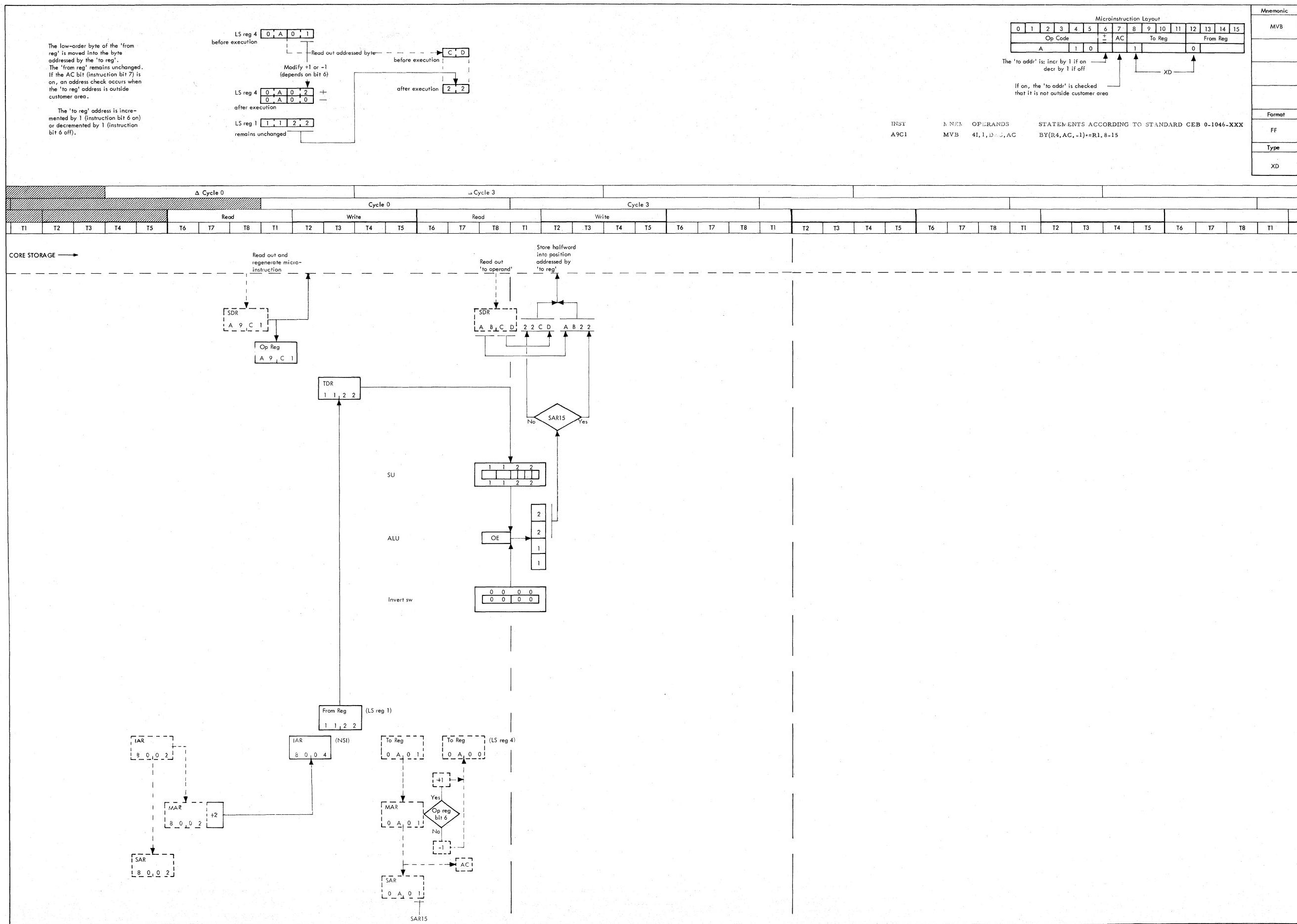
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

Diagram 5-34 Move Byte (DD) (Part 2 of 2) (03739A) 20

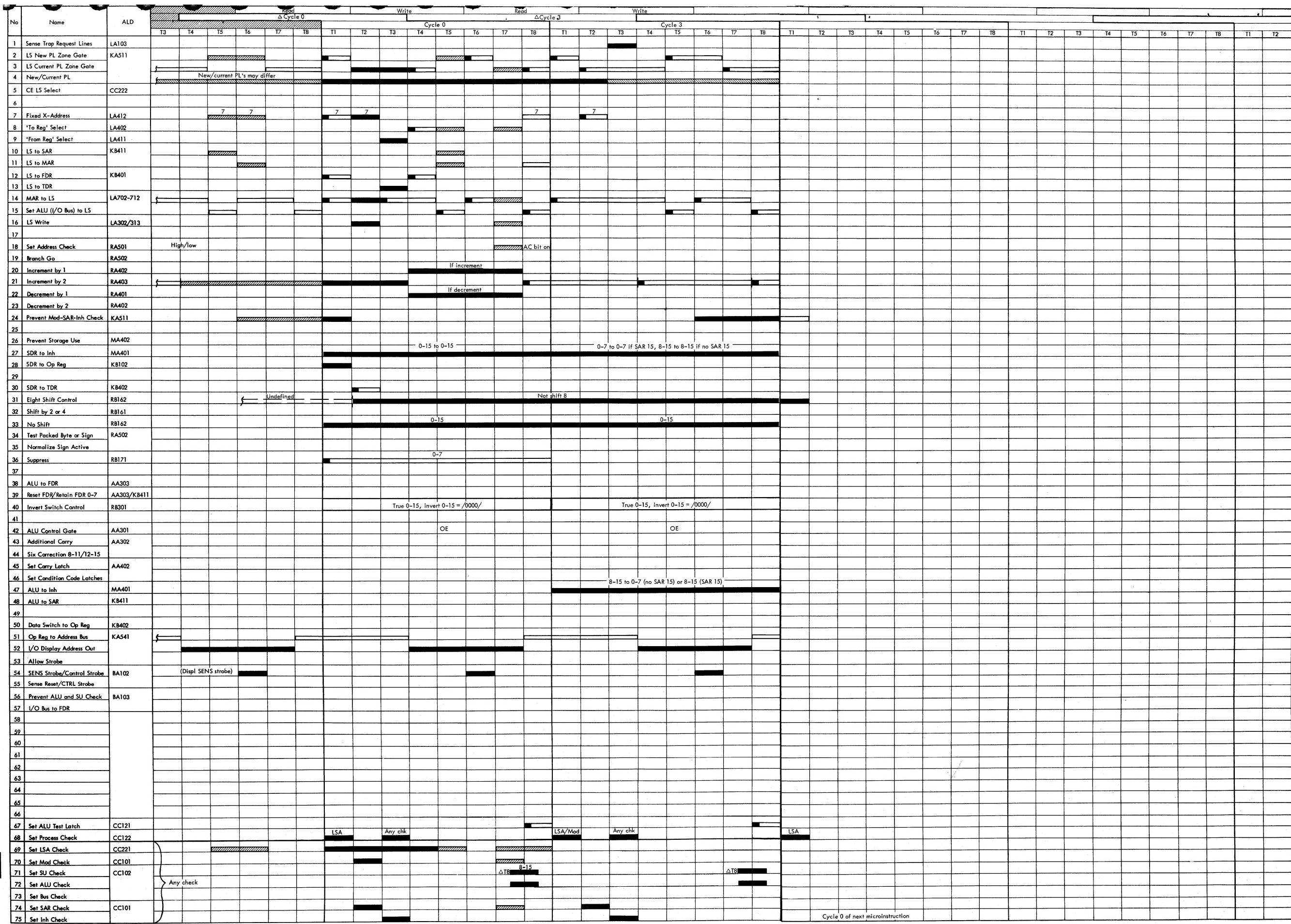


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



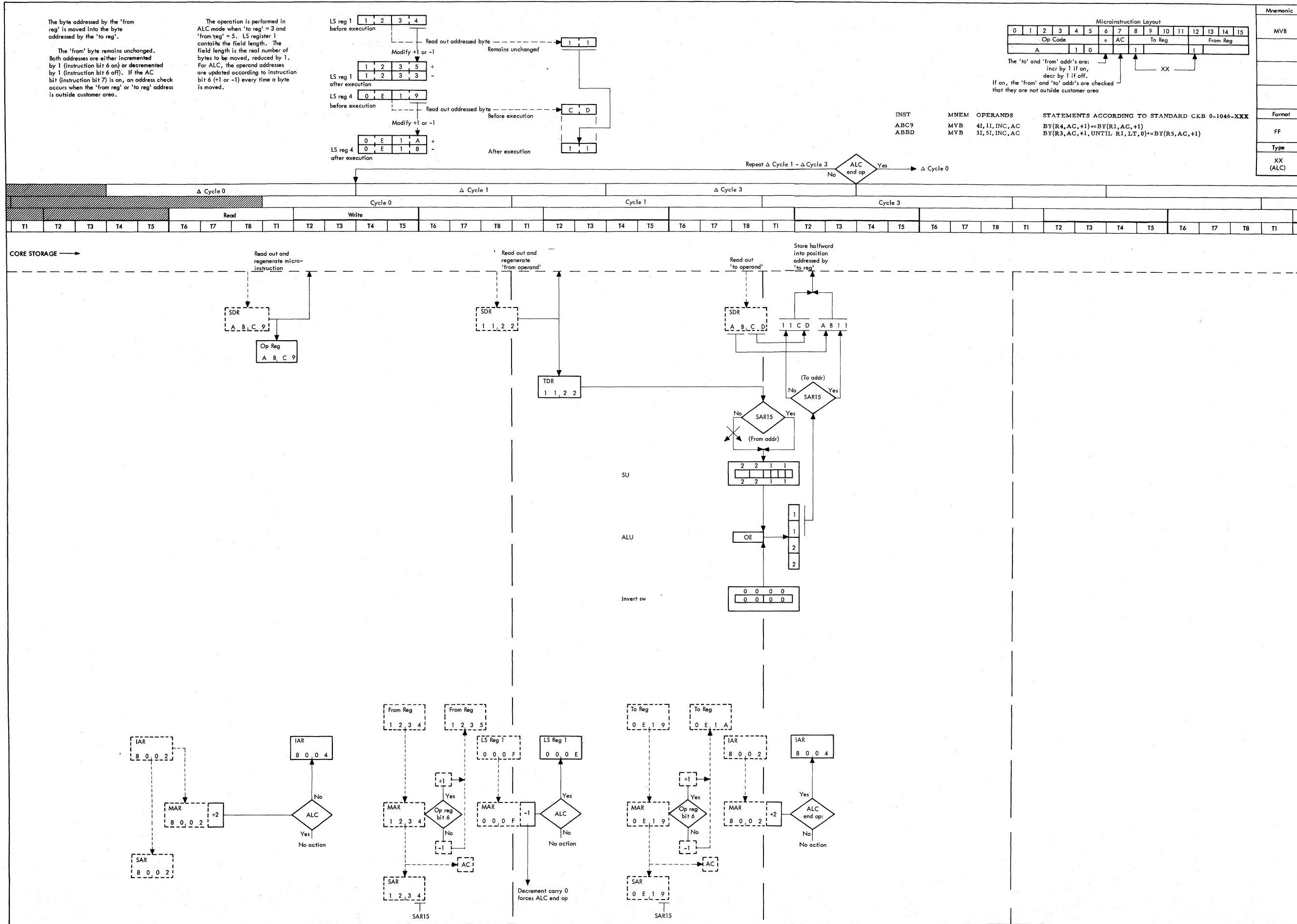


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted line.

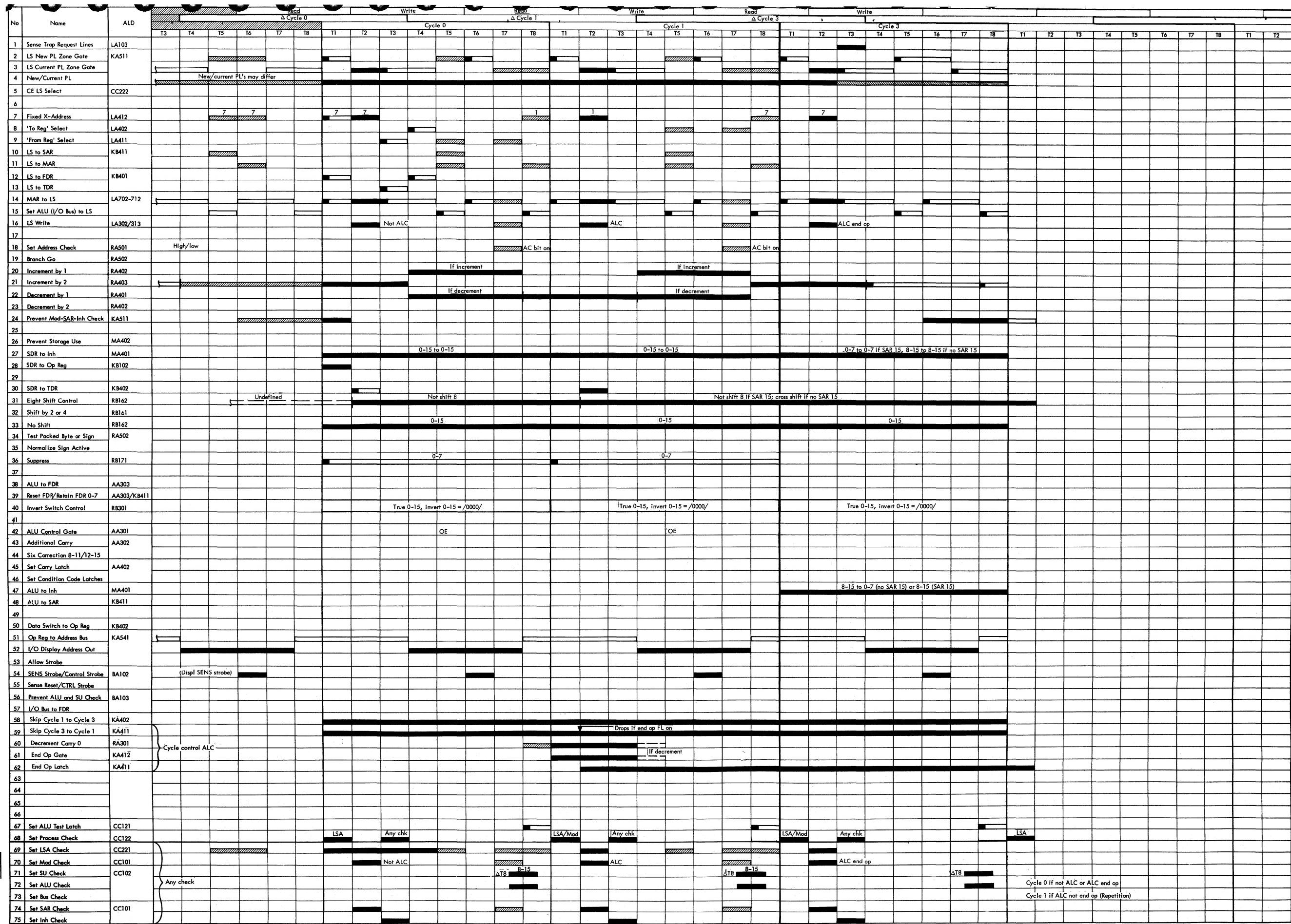


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

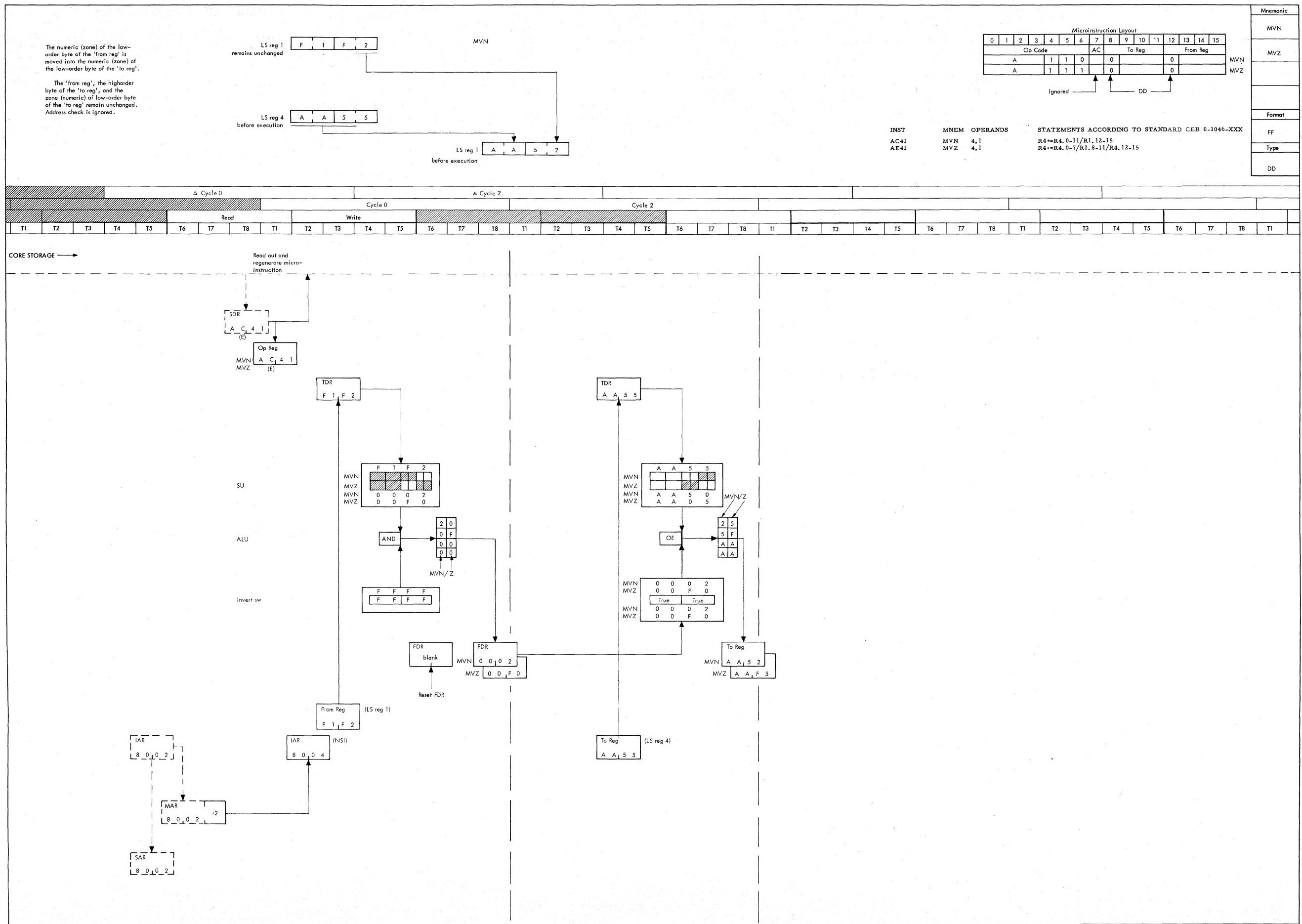


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

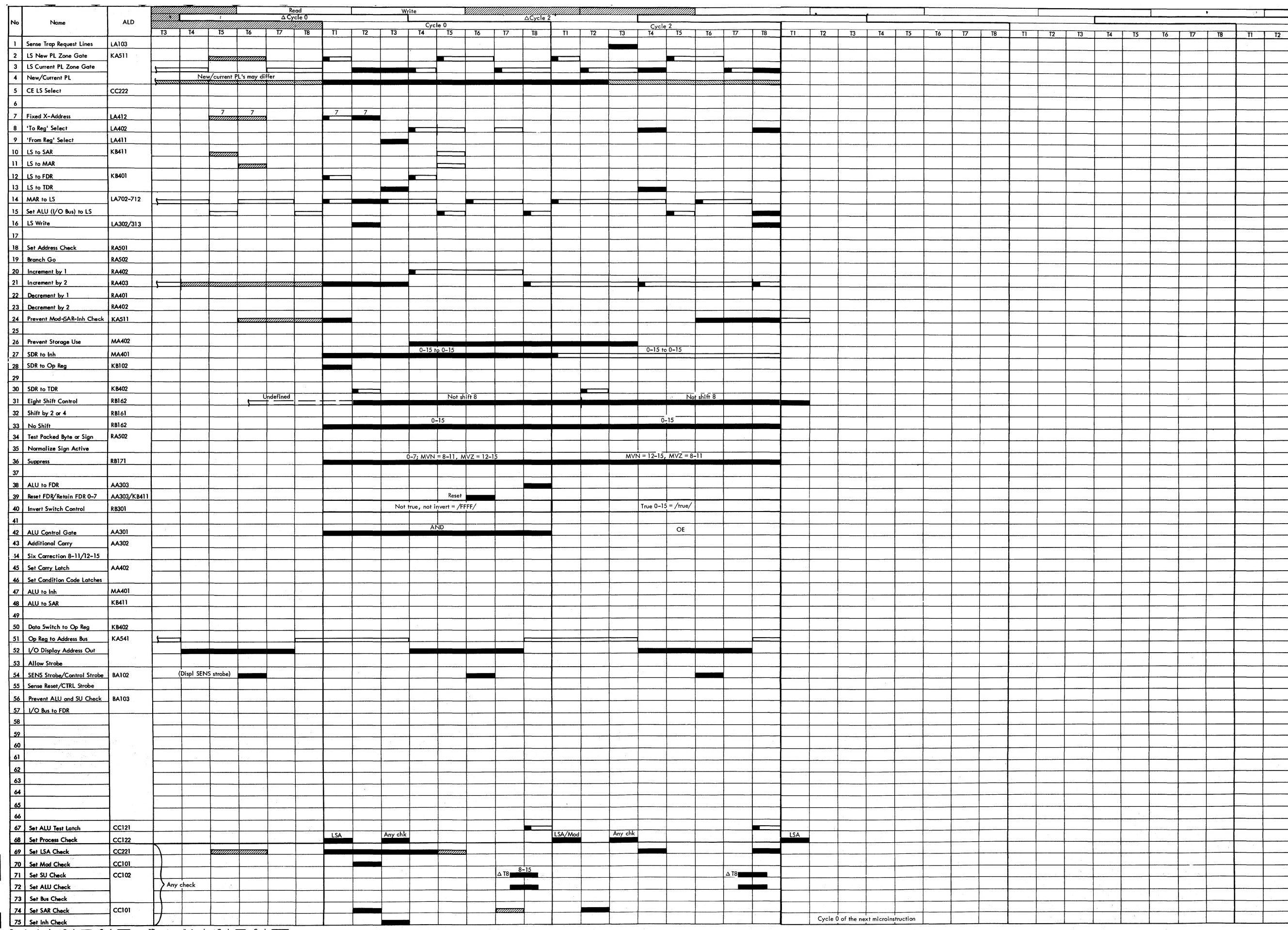


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

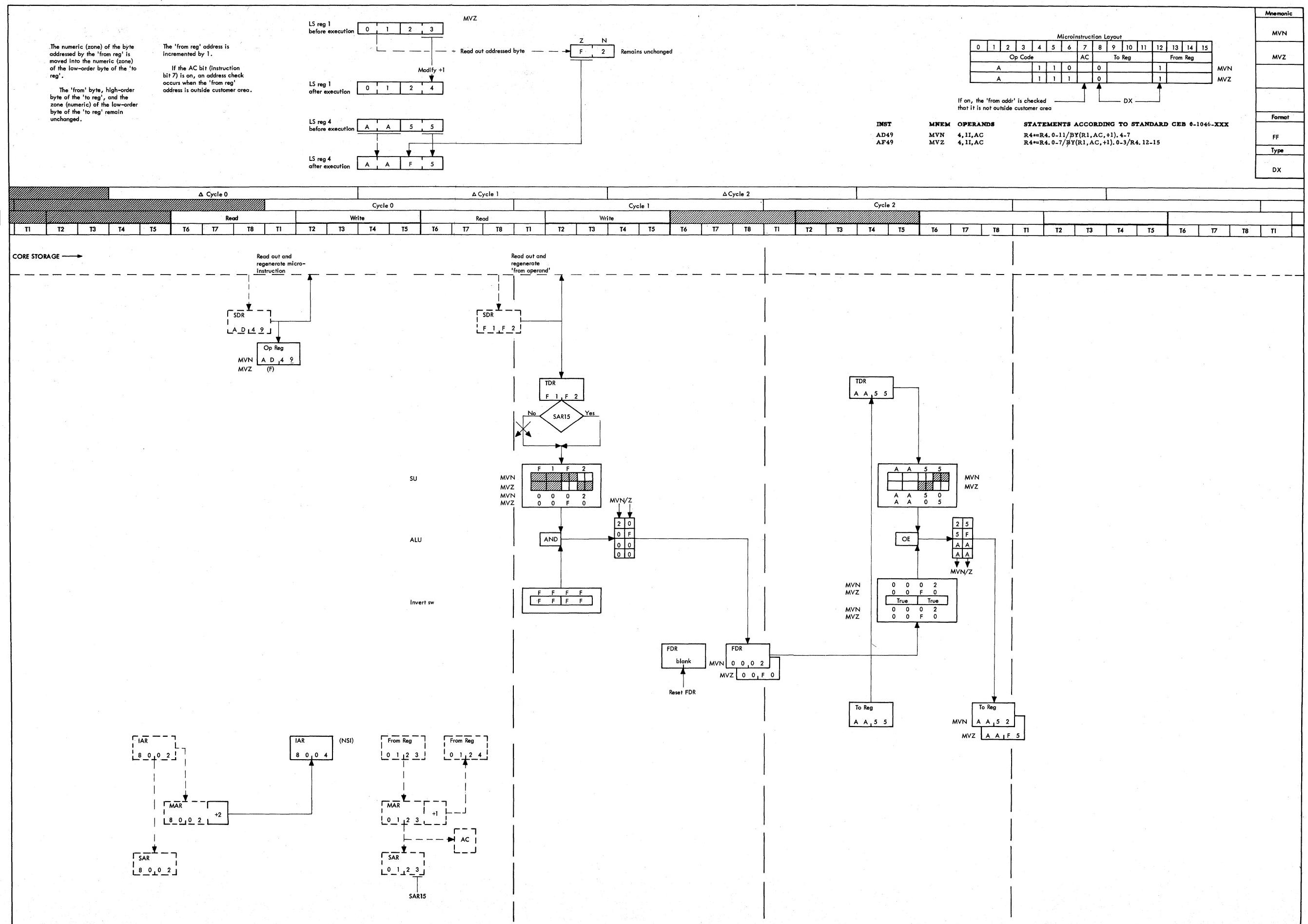


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

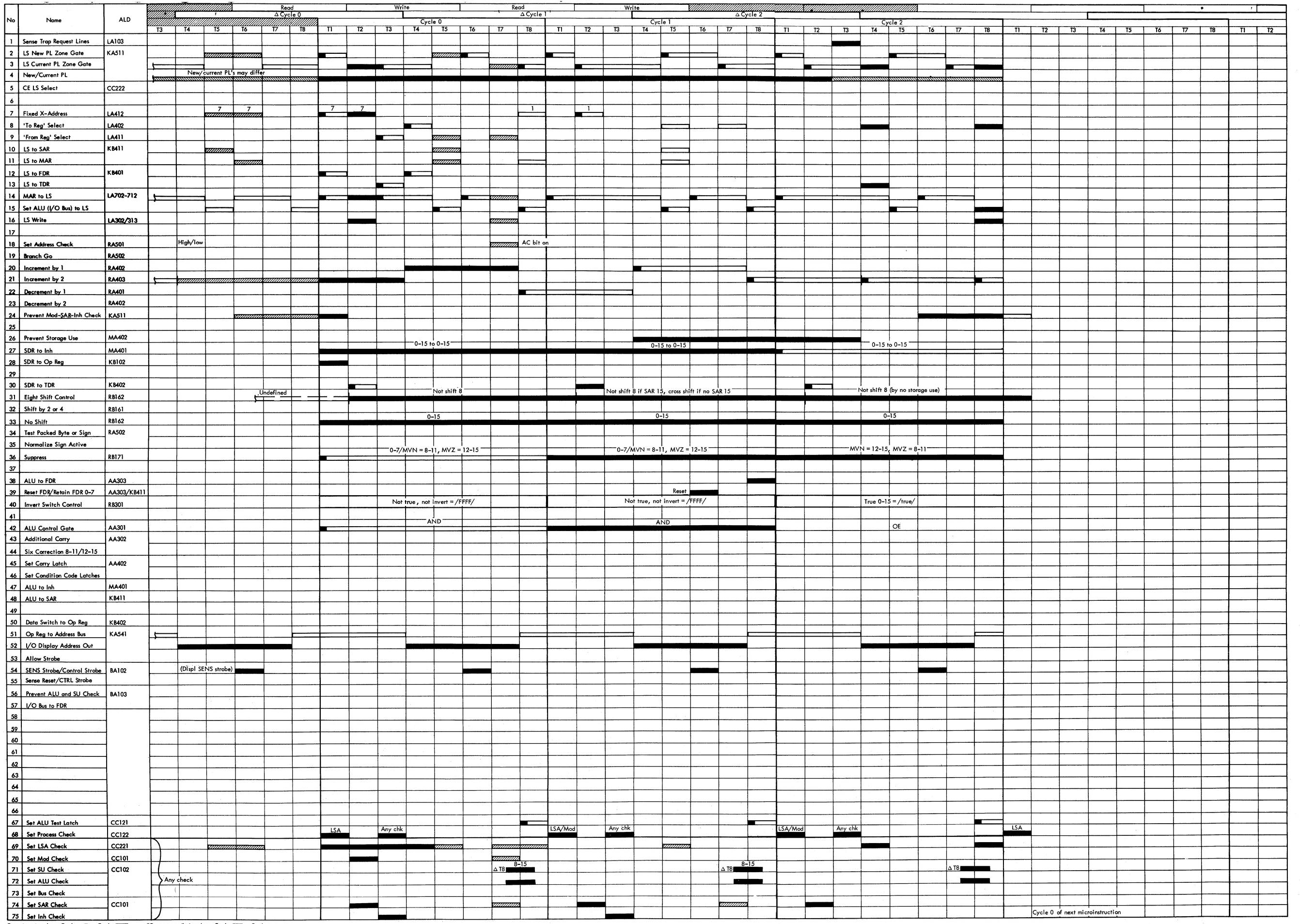


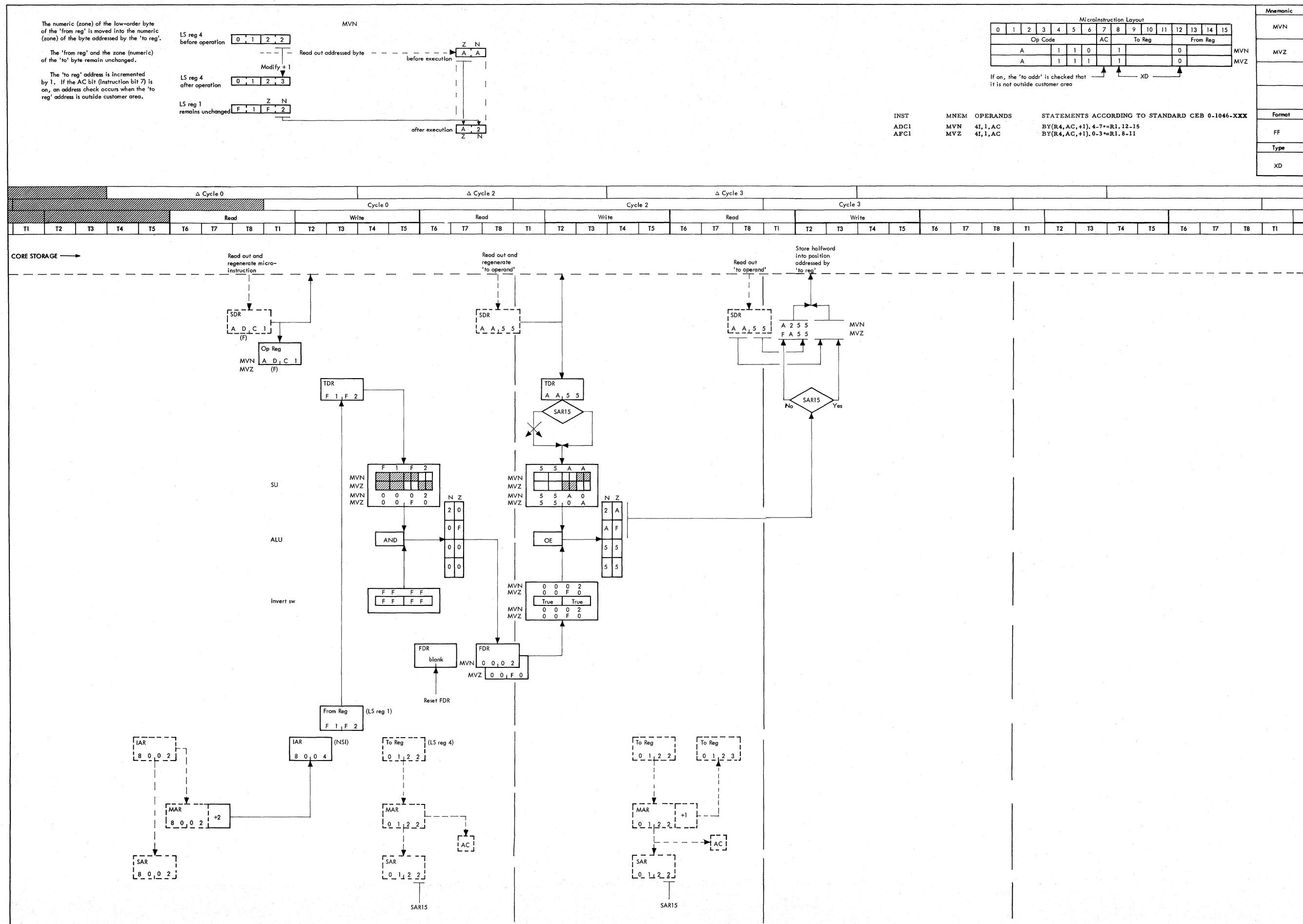
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

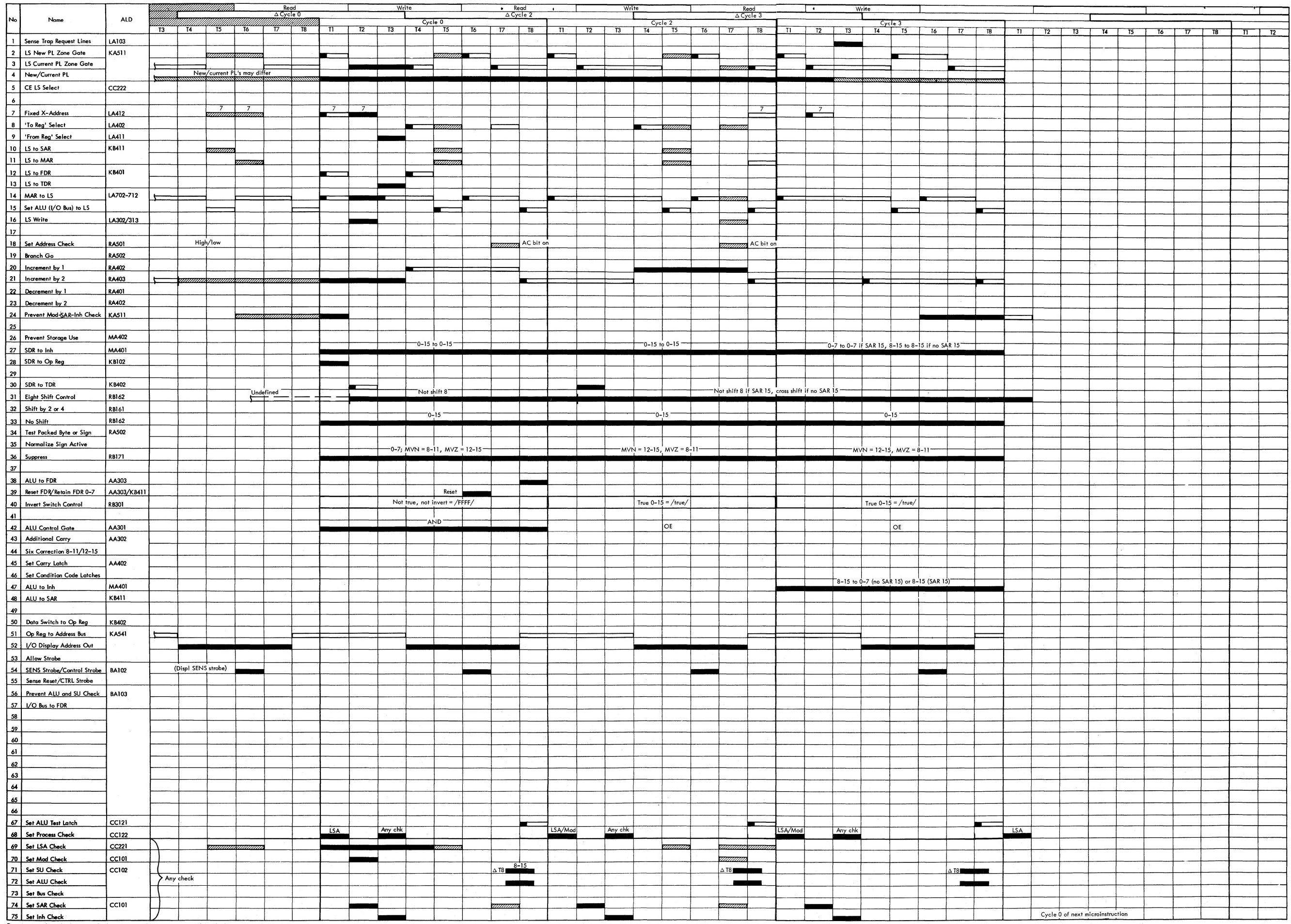


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



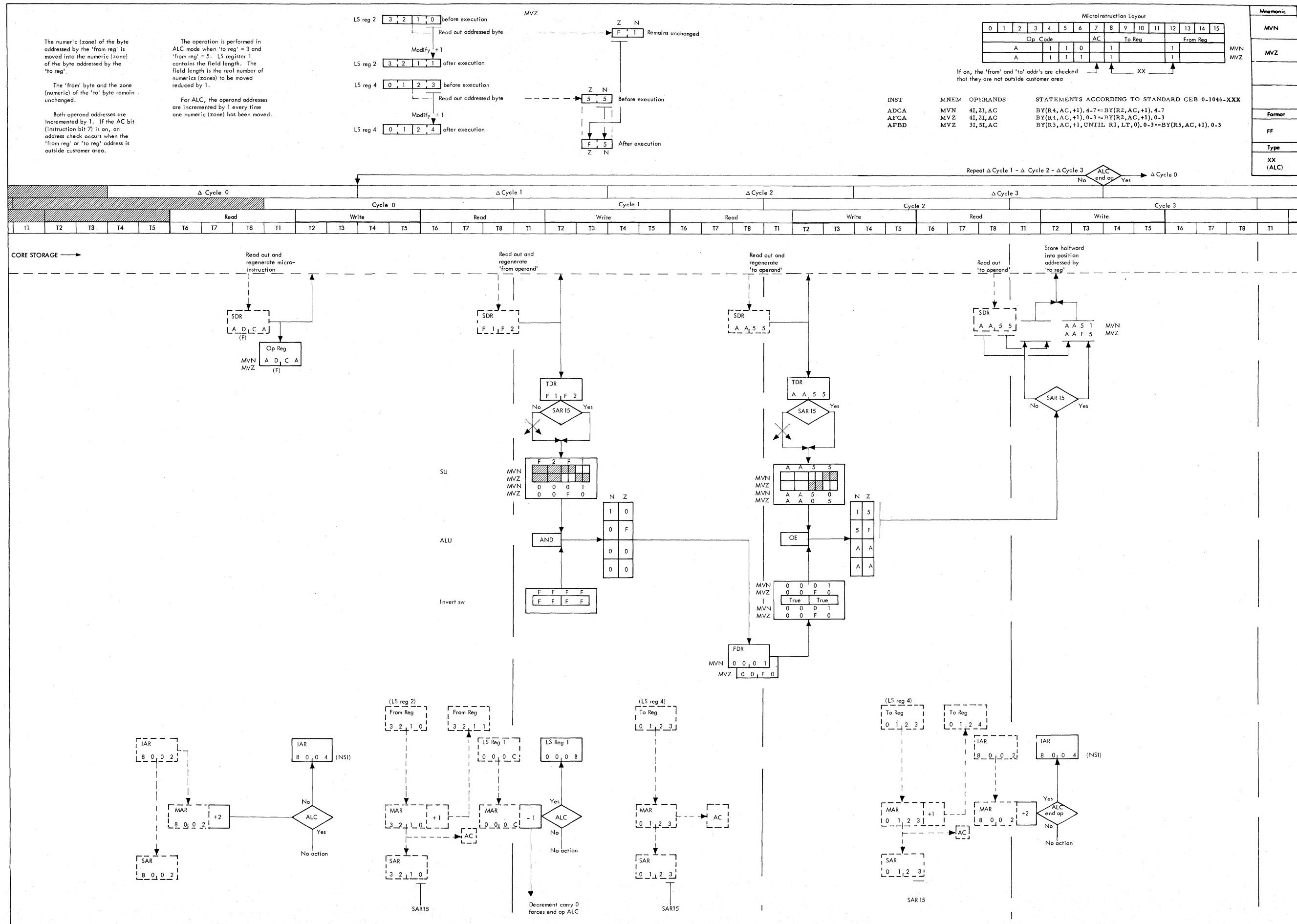


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

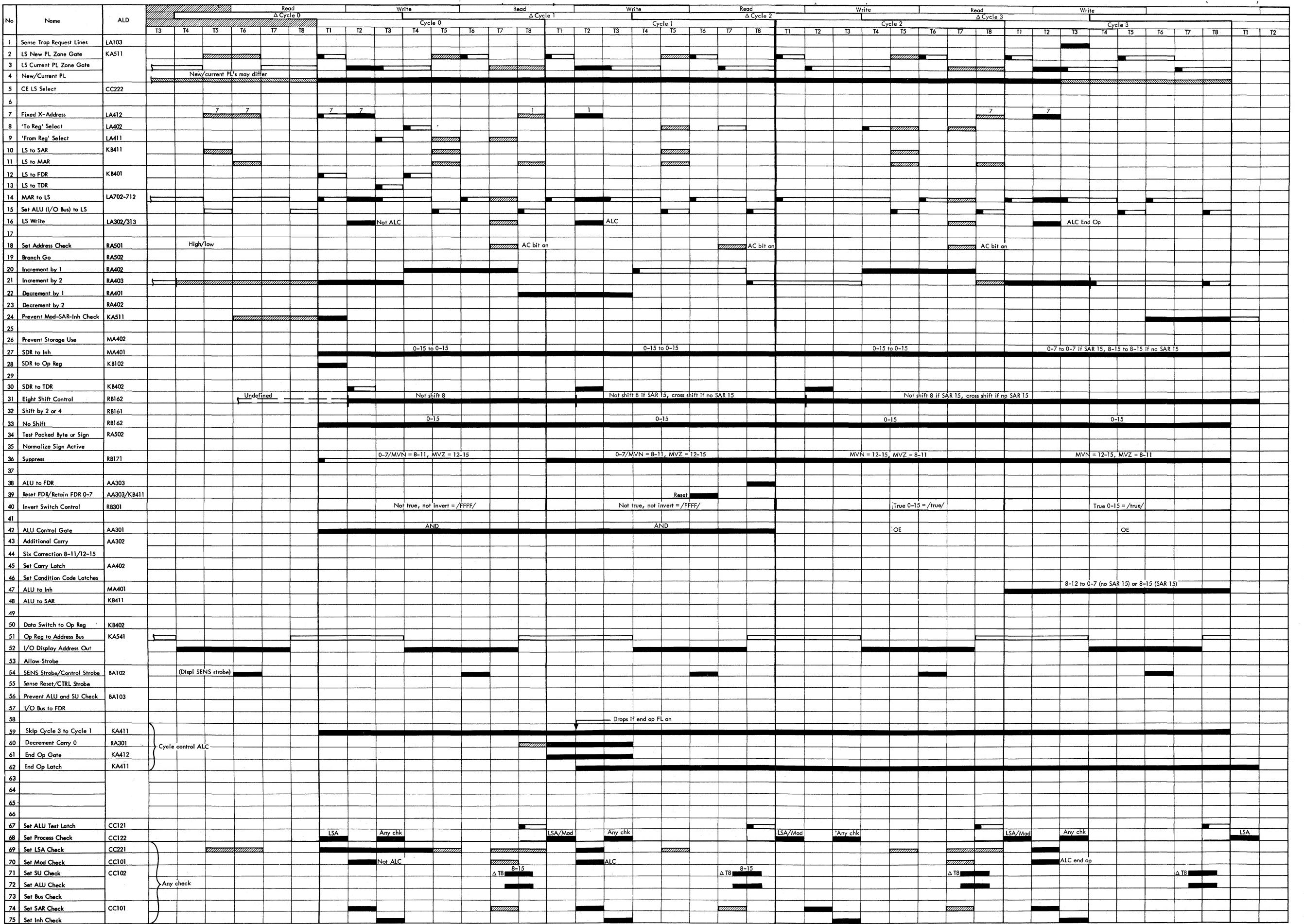


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



● Diagram 5-41. Move Numeric/Zone (XX, ALC) (Part 2 of 2) (03746A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

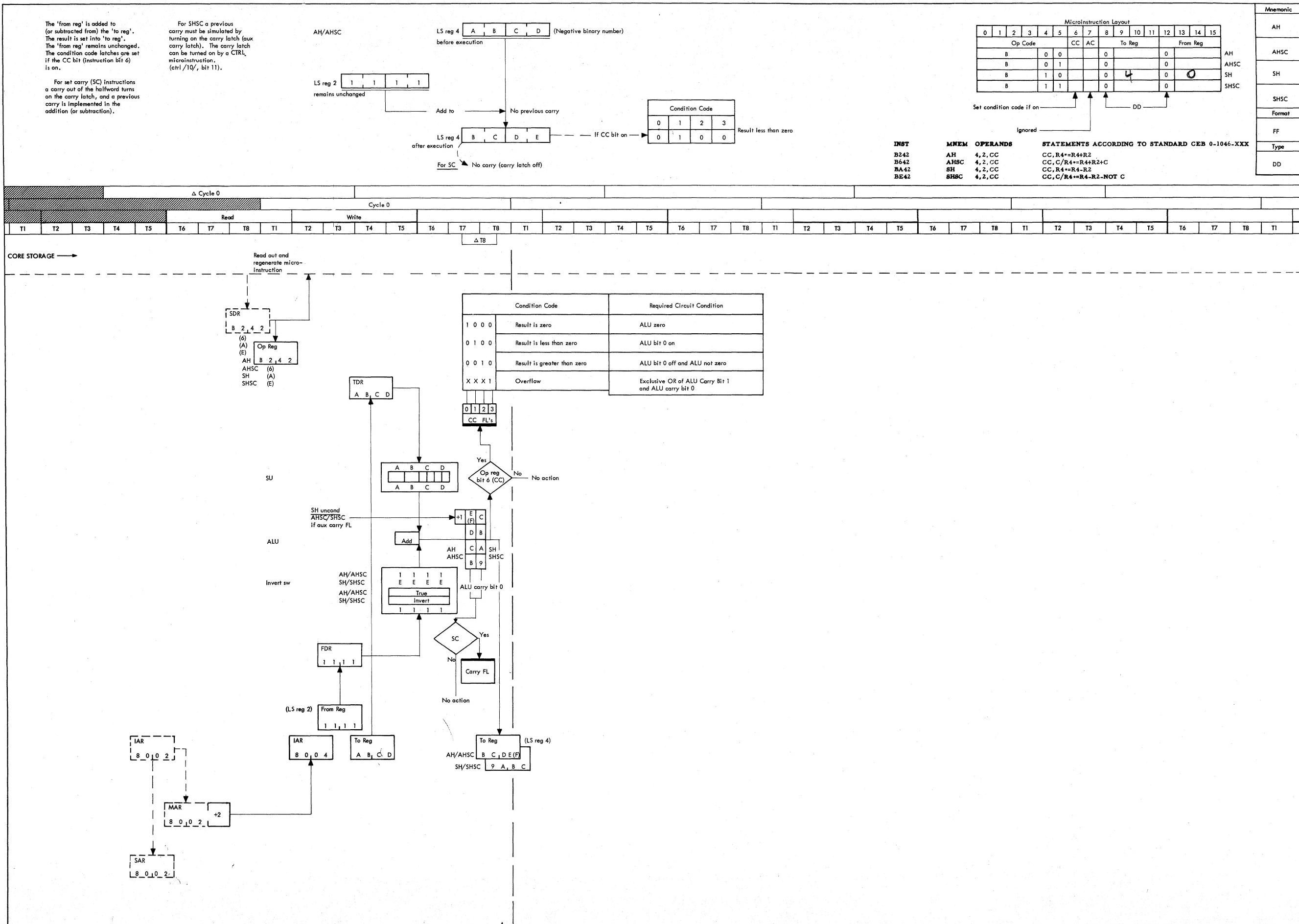


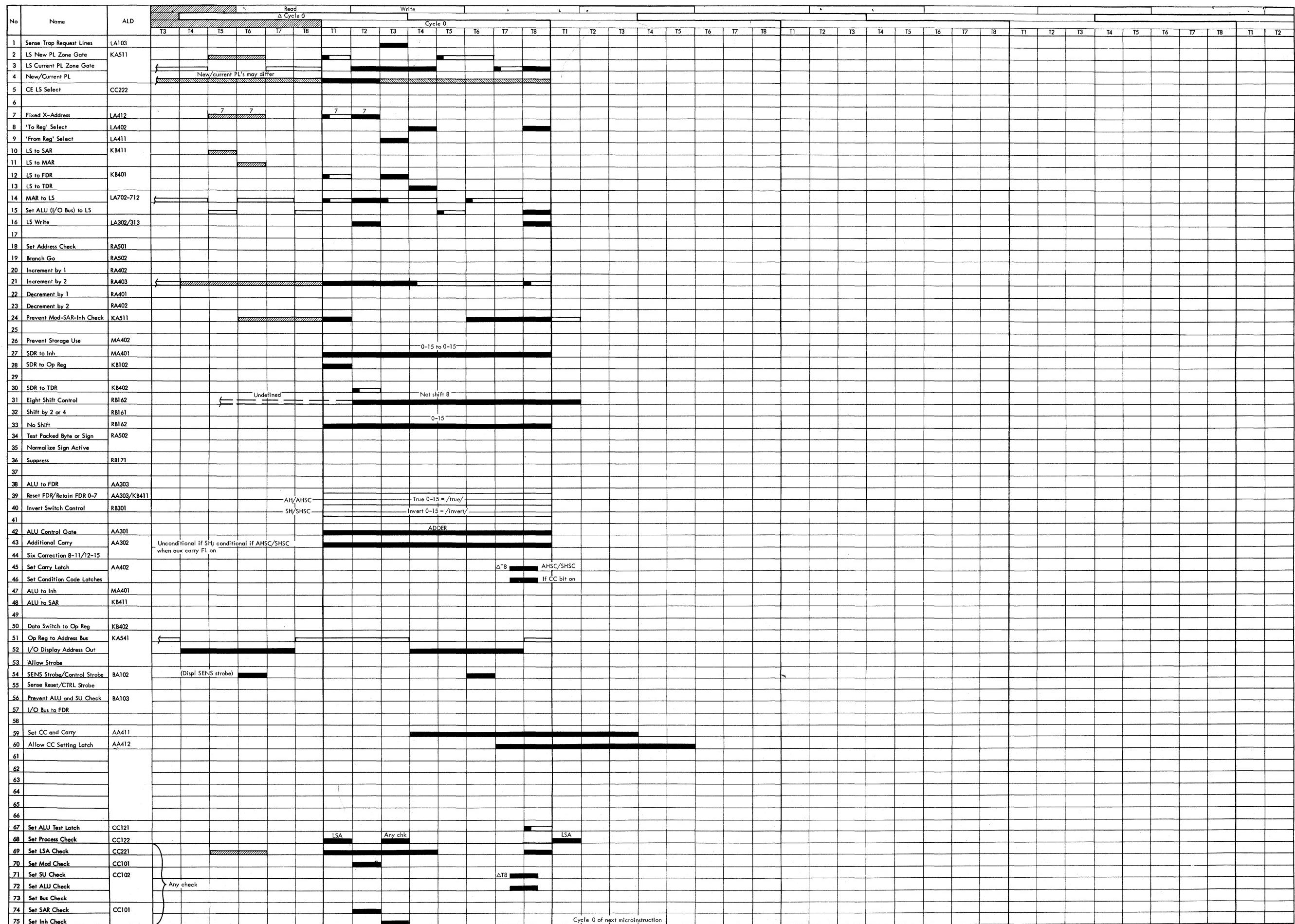
Diagram 5-42. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (DD) (Part 1 of 2) (03747A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Note: For "Do not care" functions refer to timing chart below.

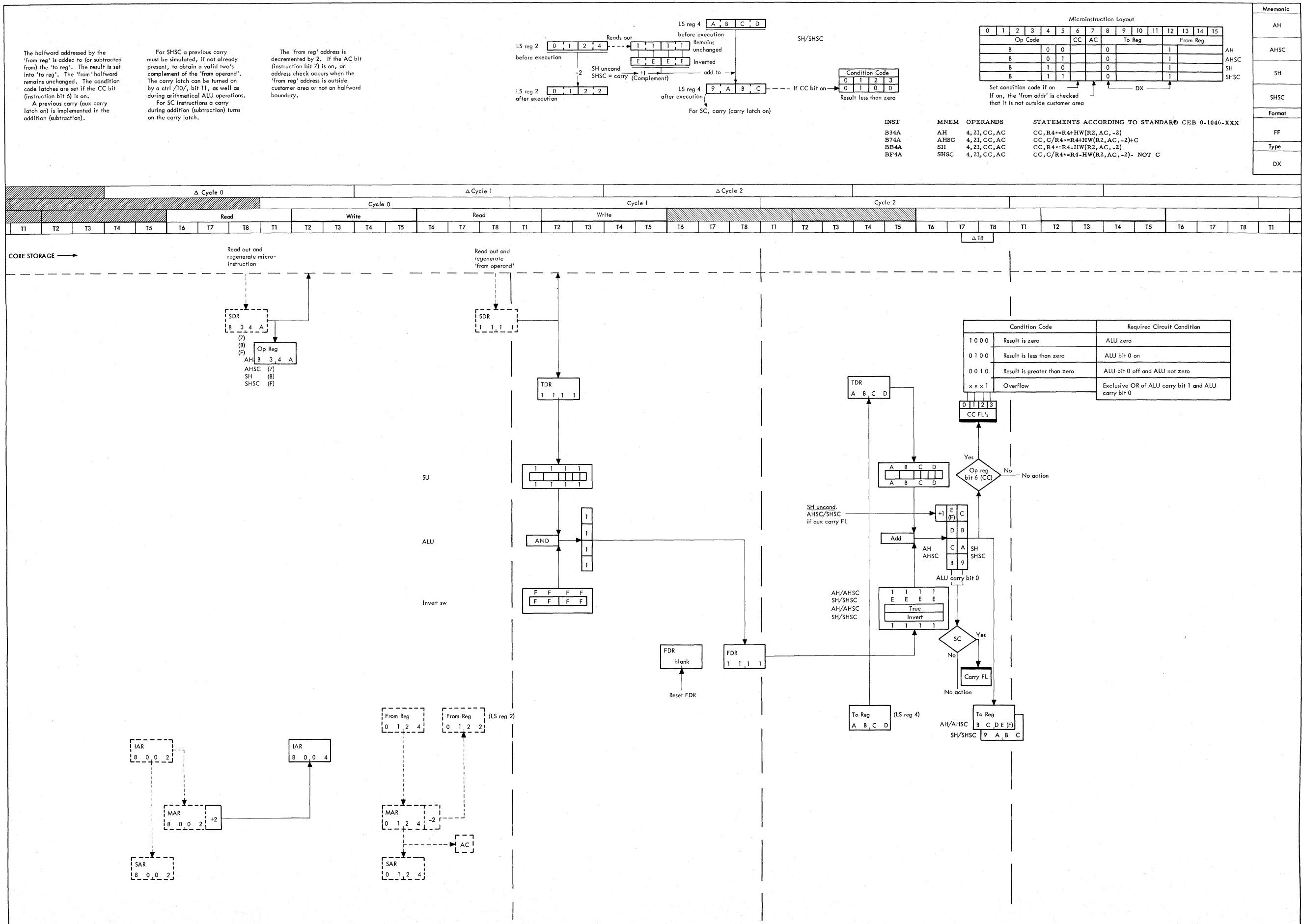
"Do not care" signals:

Δ Cycle []

Cycle []



Function signals: ΔCycle Cycle "Do not care" signals: ΔCycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

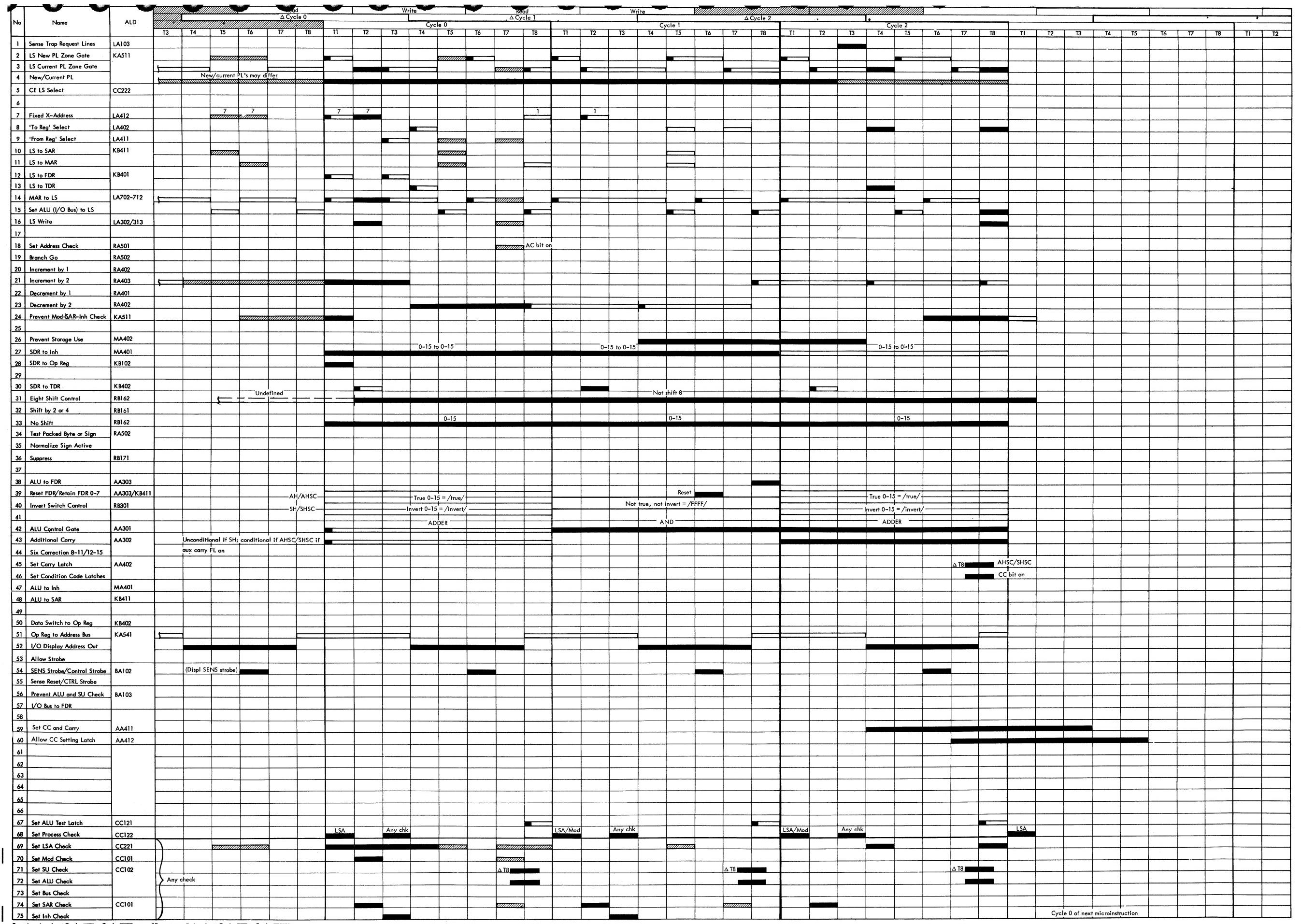
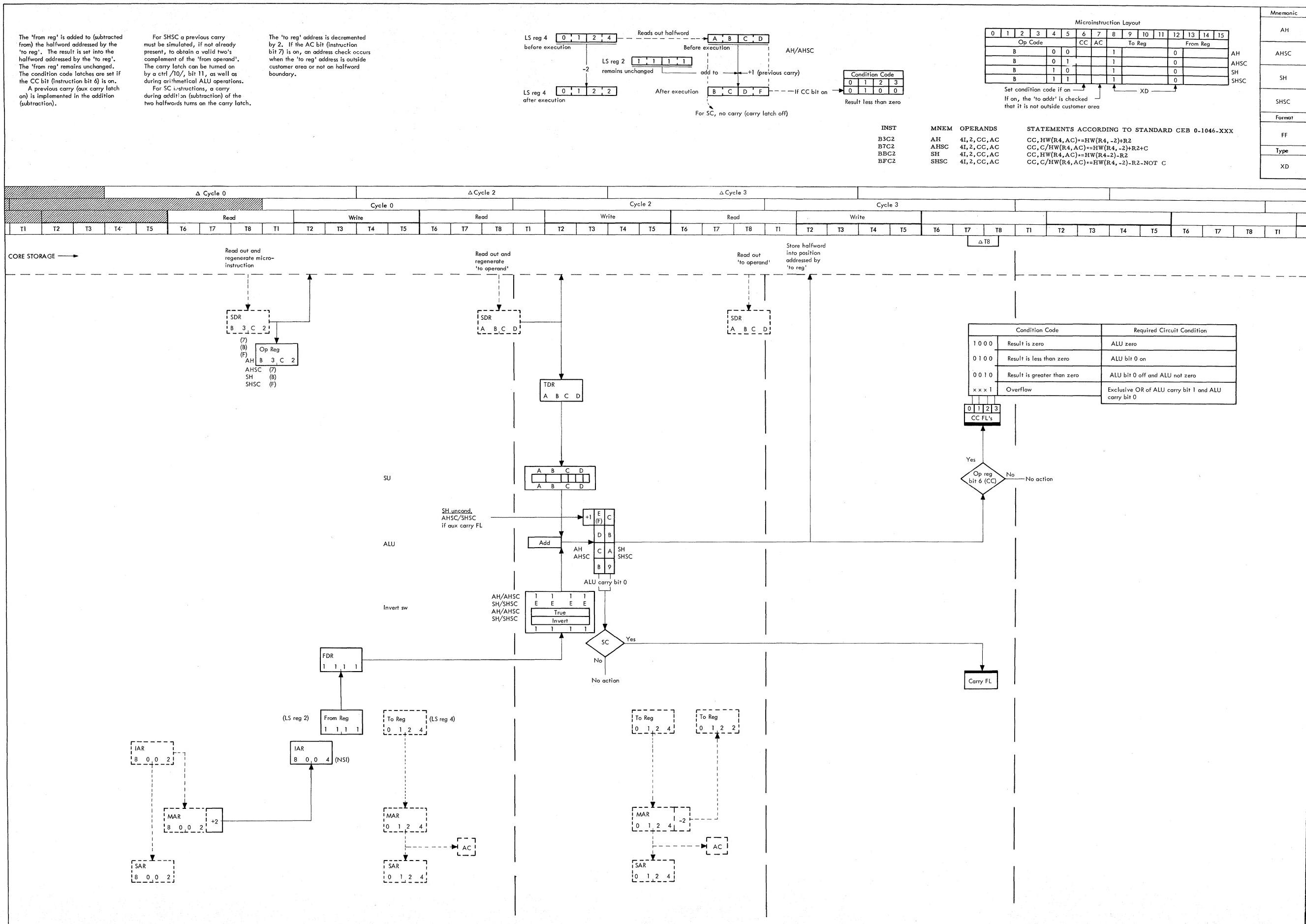
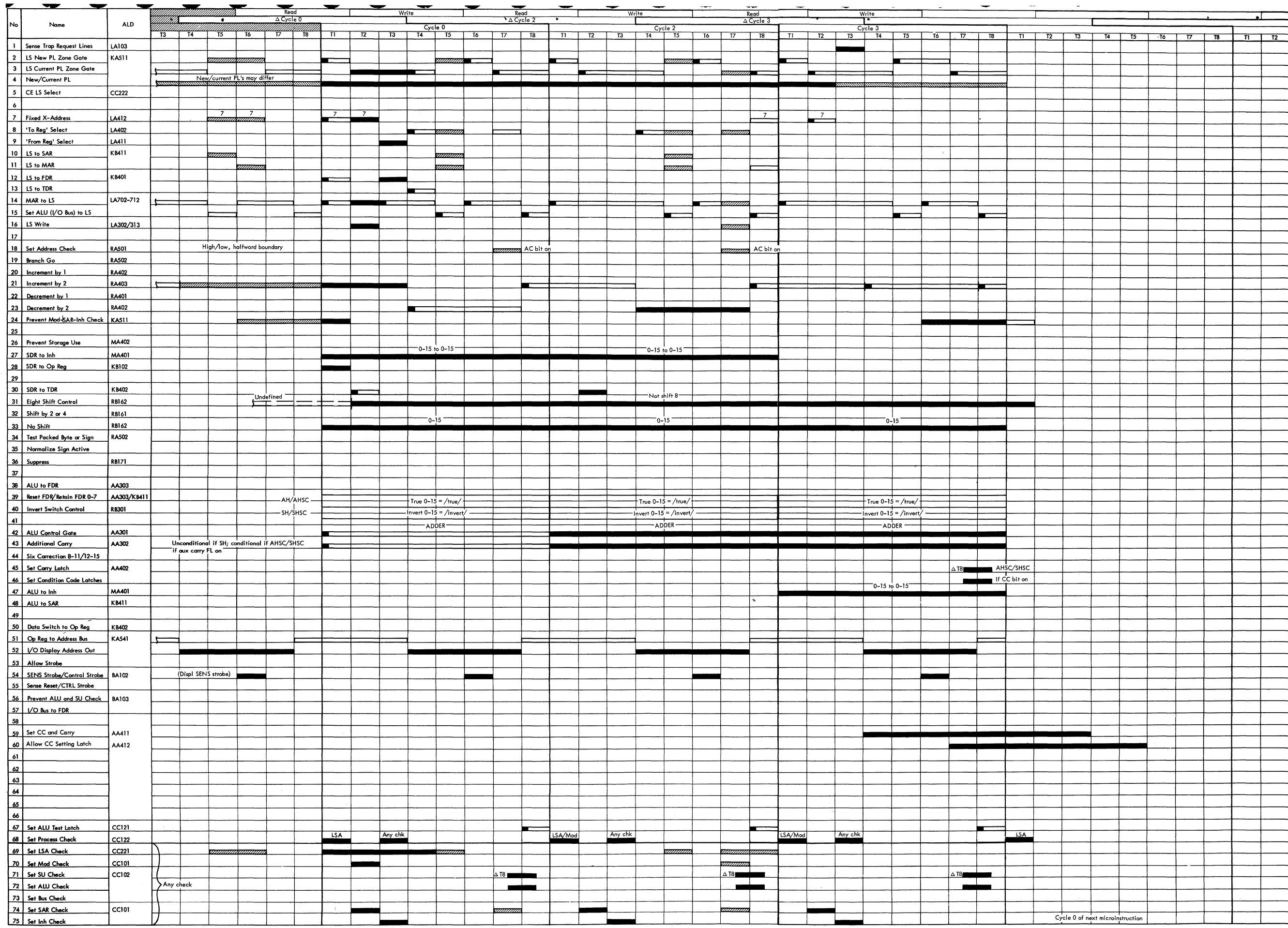
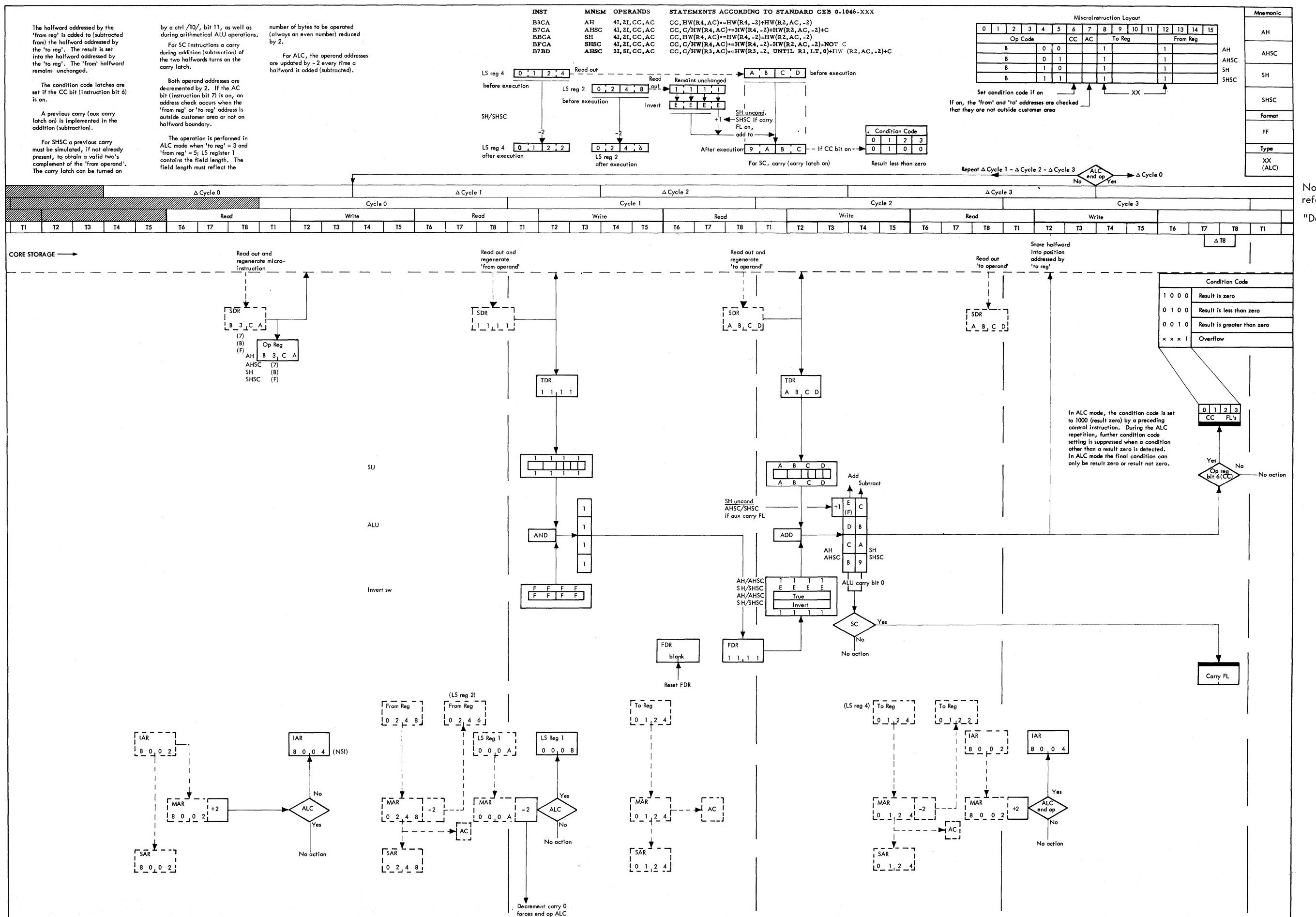


Diagram 5-43. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (DX) (Part 2 of 2) (03748A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)



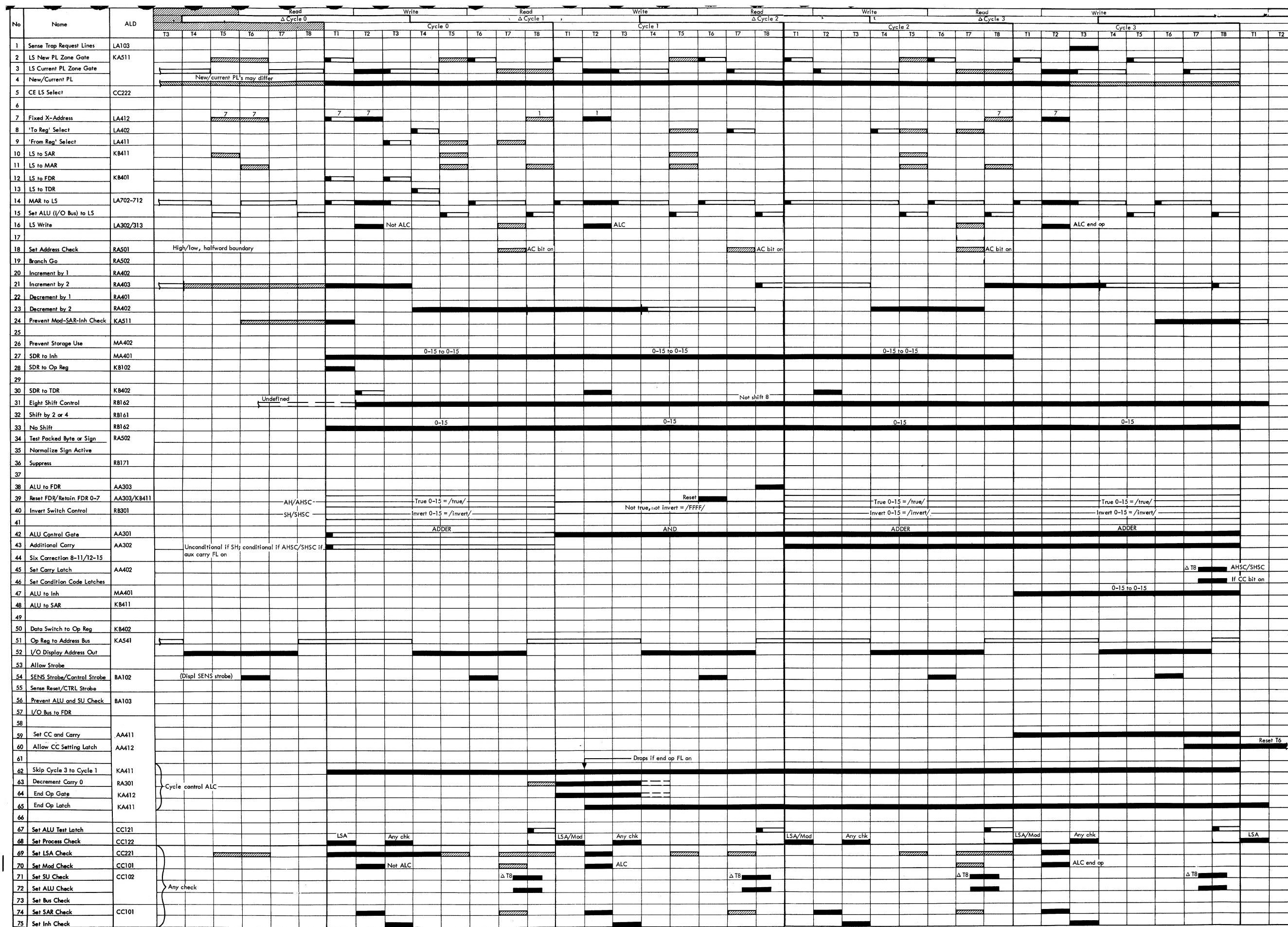
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.





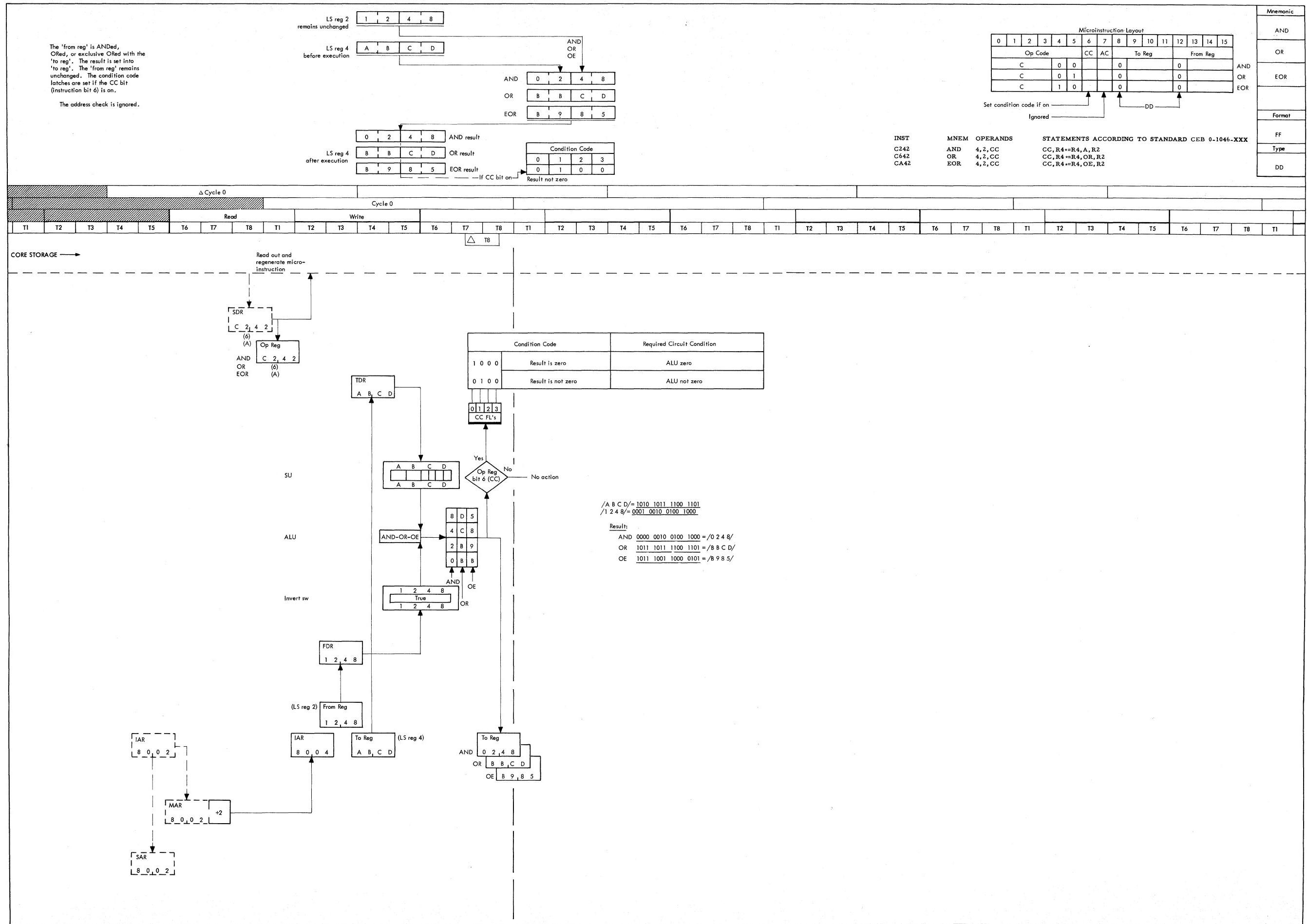
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

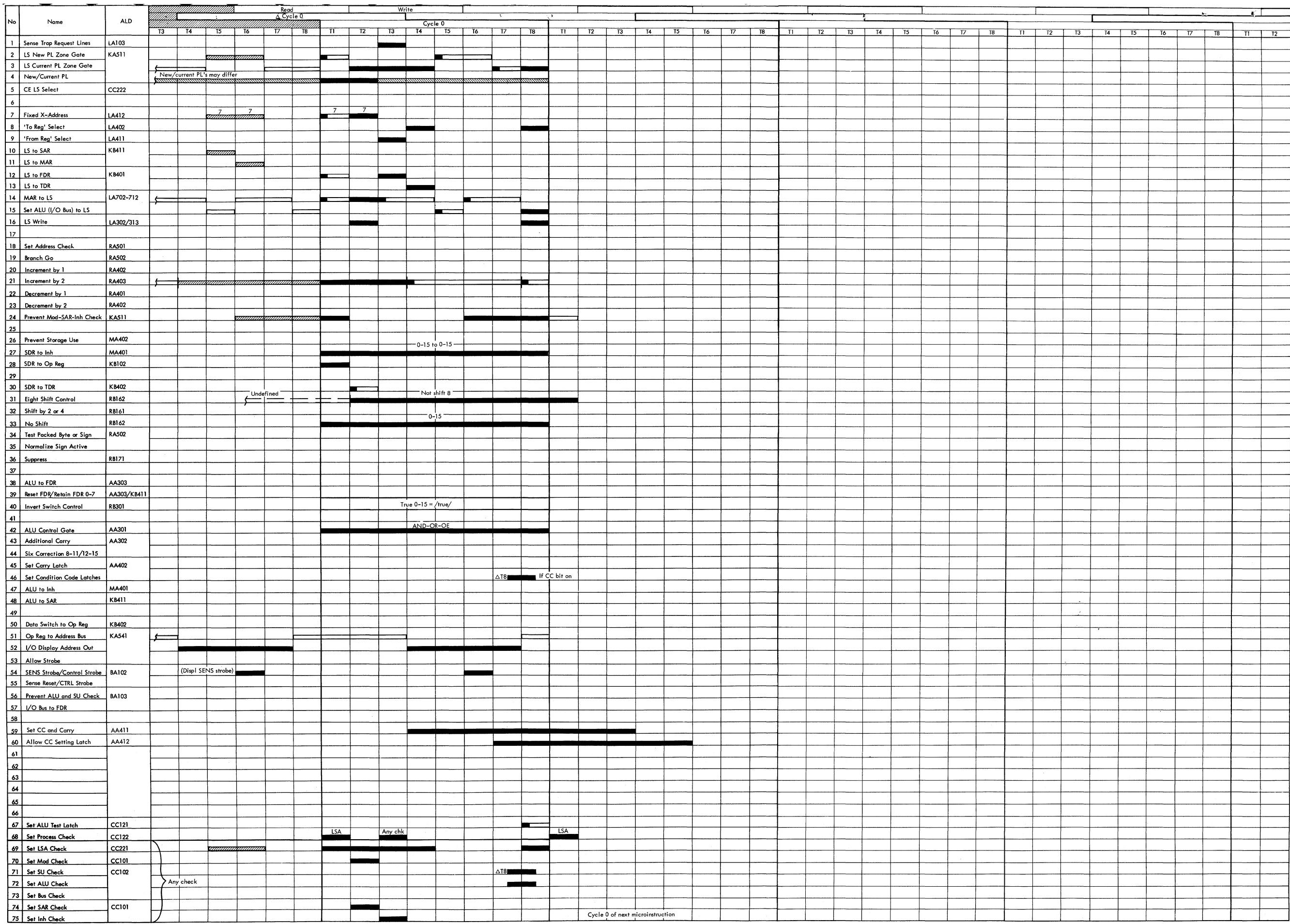
Diagram 5-45. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (XX, ALC) (Part 1 of 2)



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

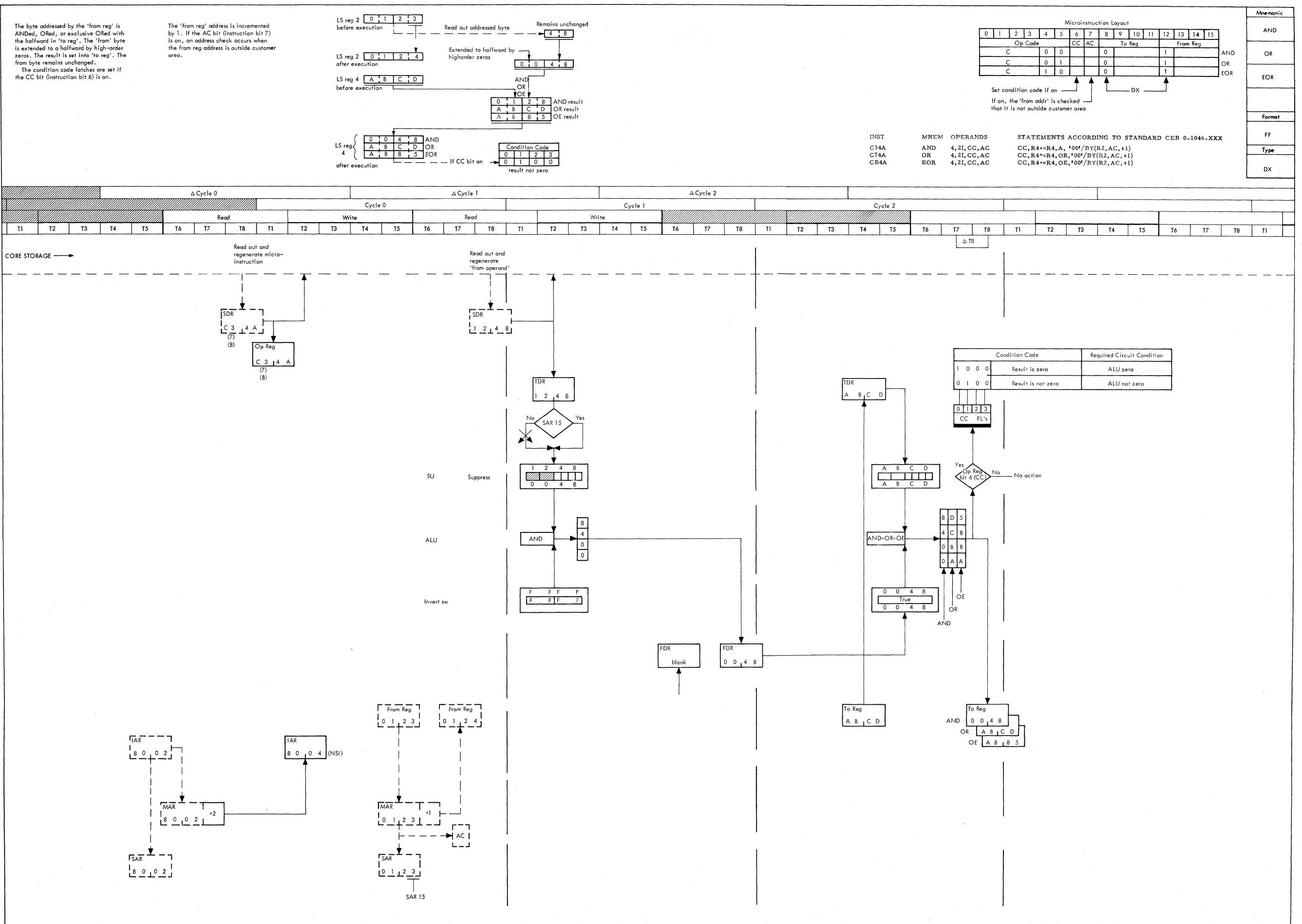
"Do not care" signals: Δ Cycle Cycle



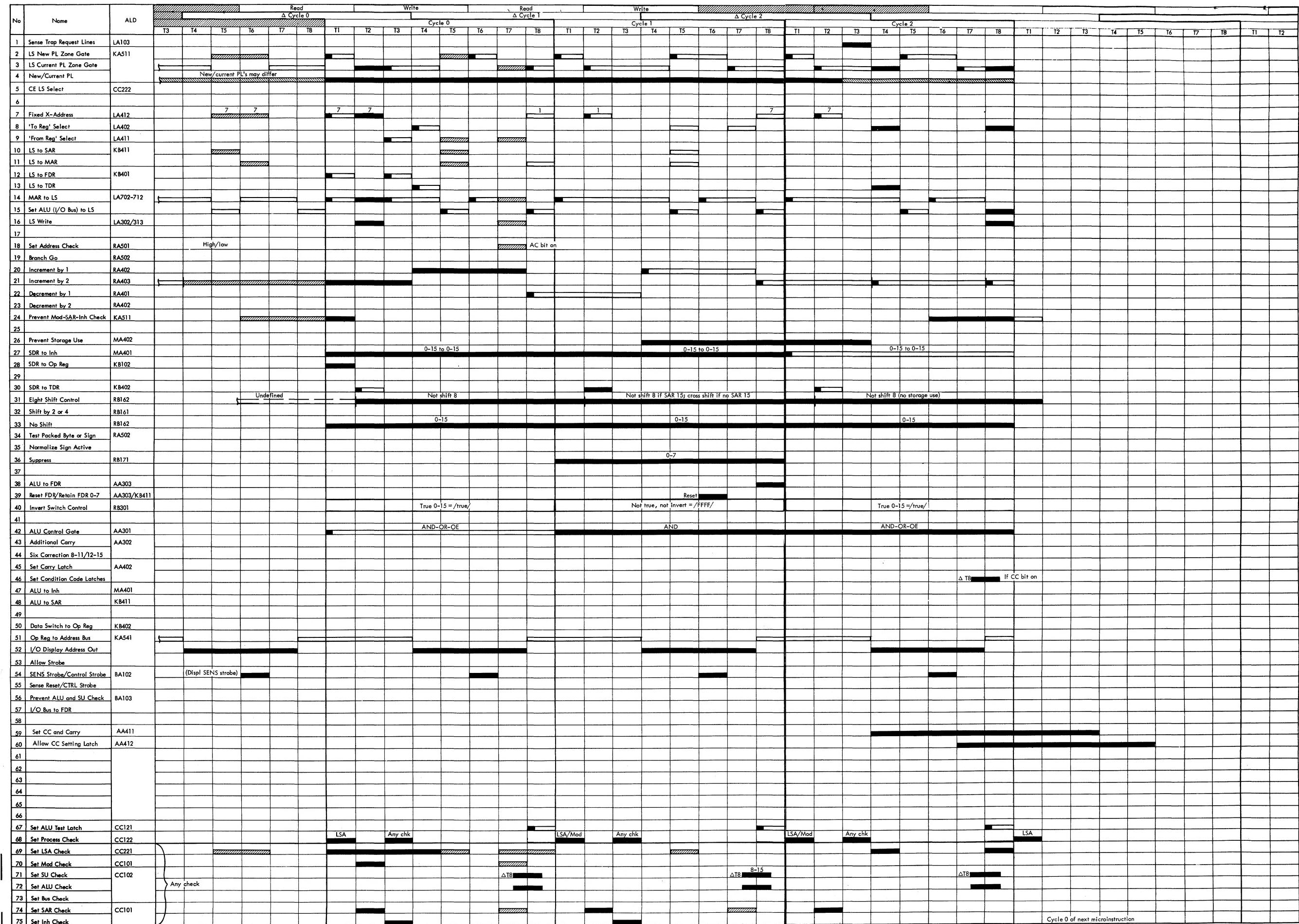


Function signals: △Cycle Cycle

"Do not care" signals: △Cycle Cycle

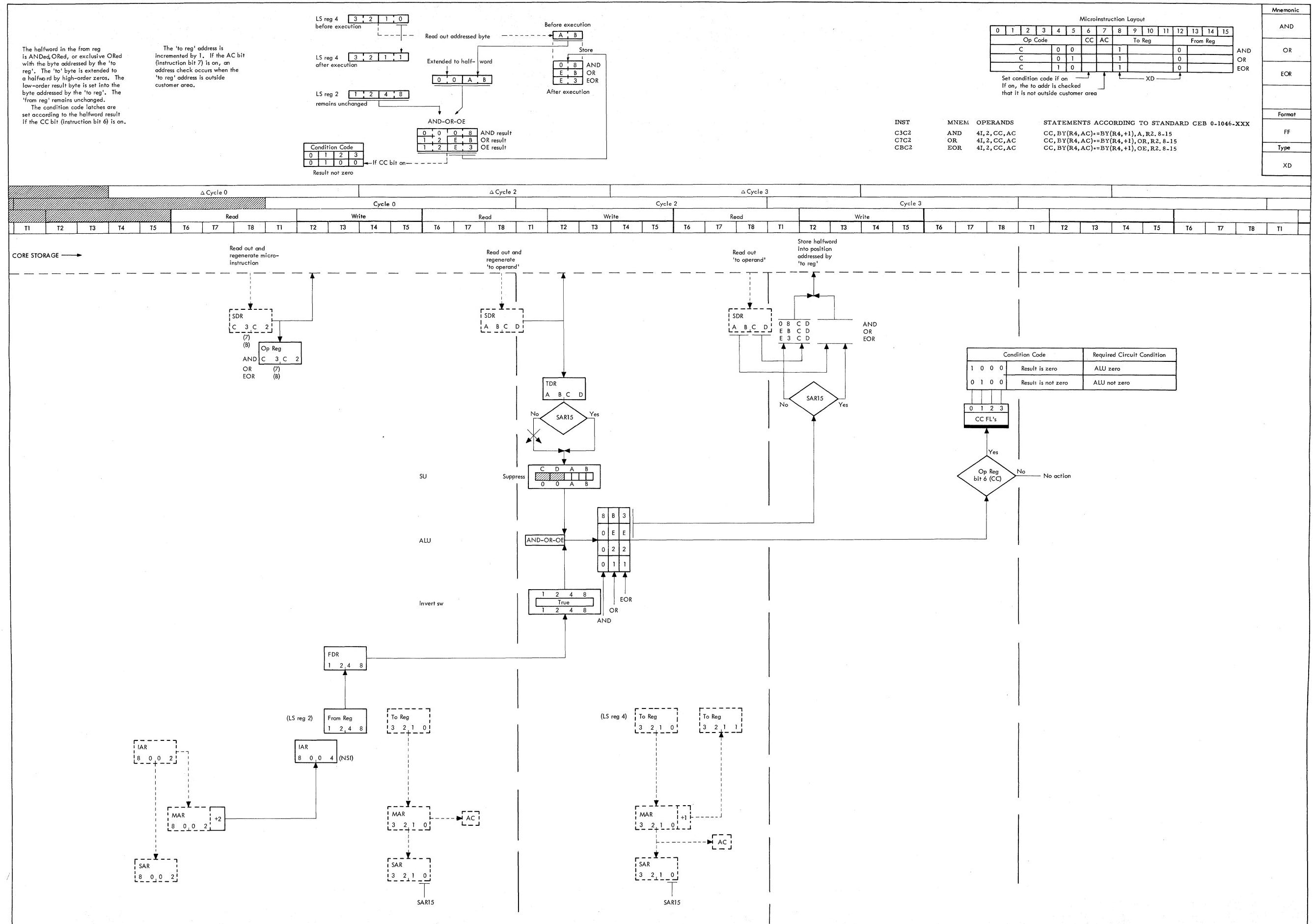


Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

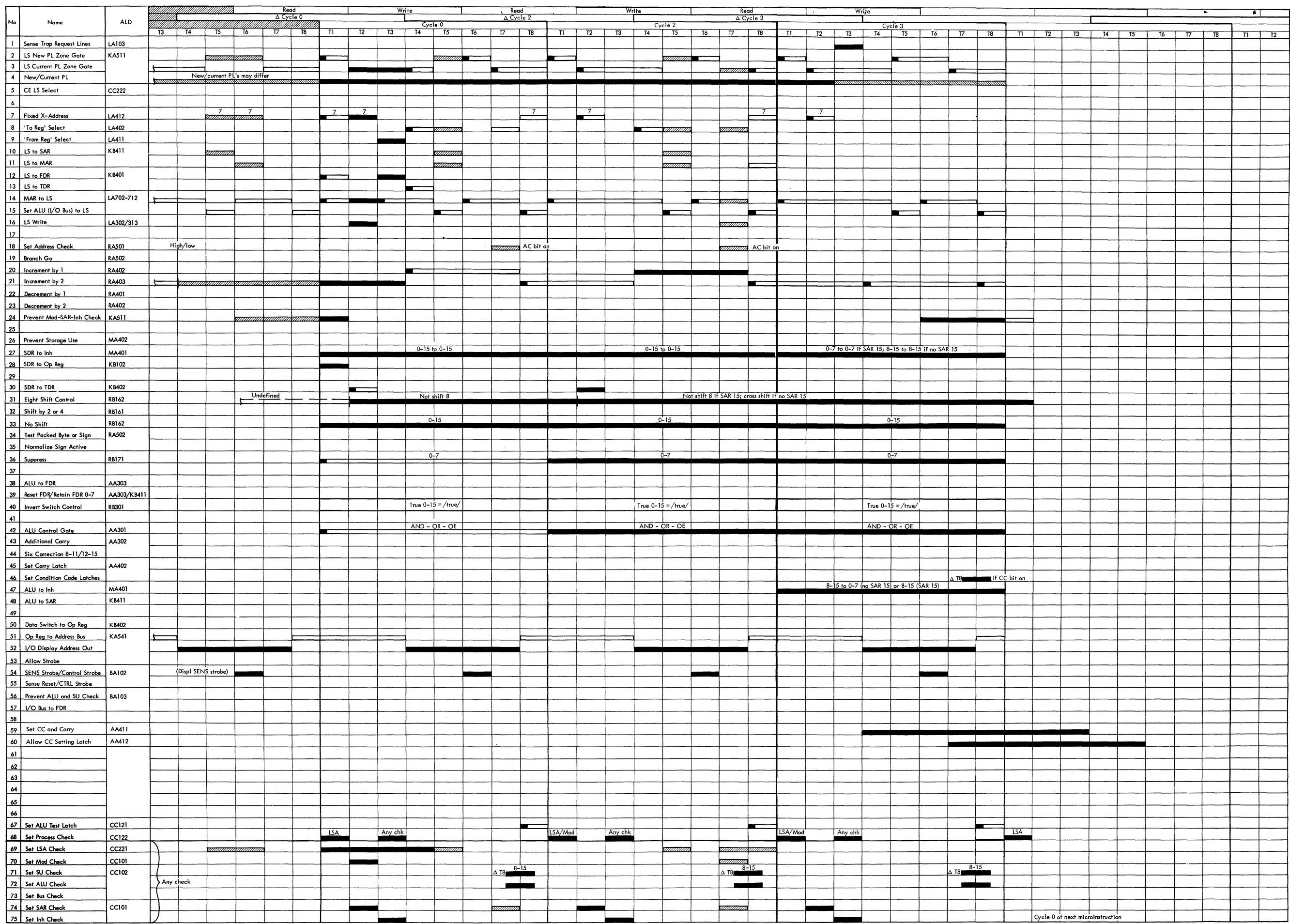


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: ΔCycle Cycle

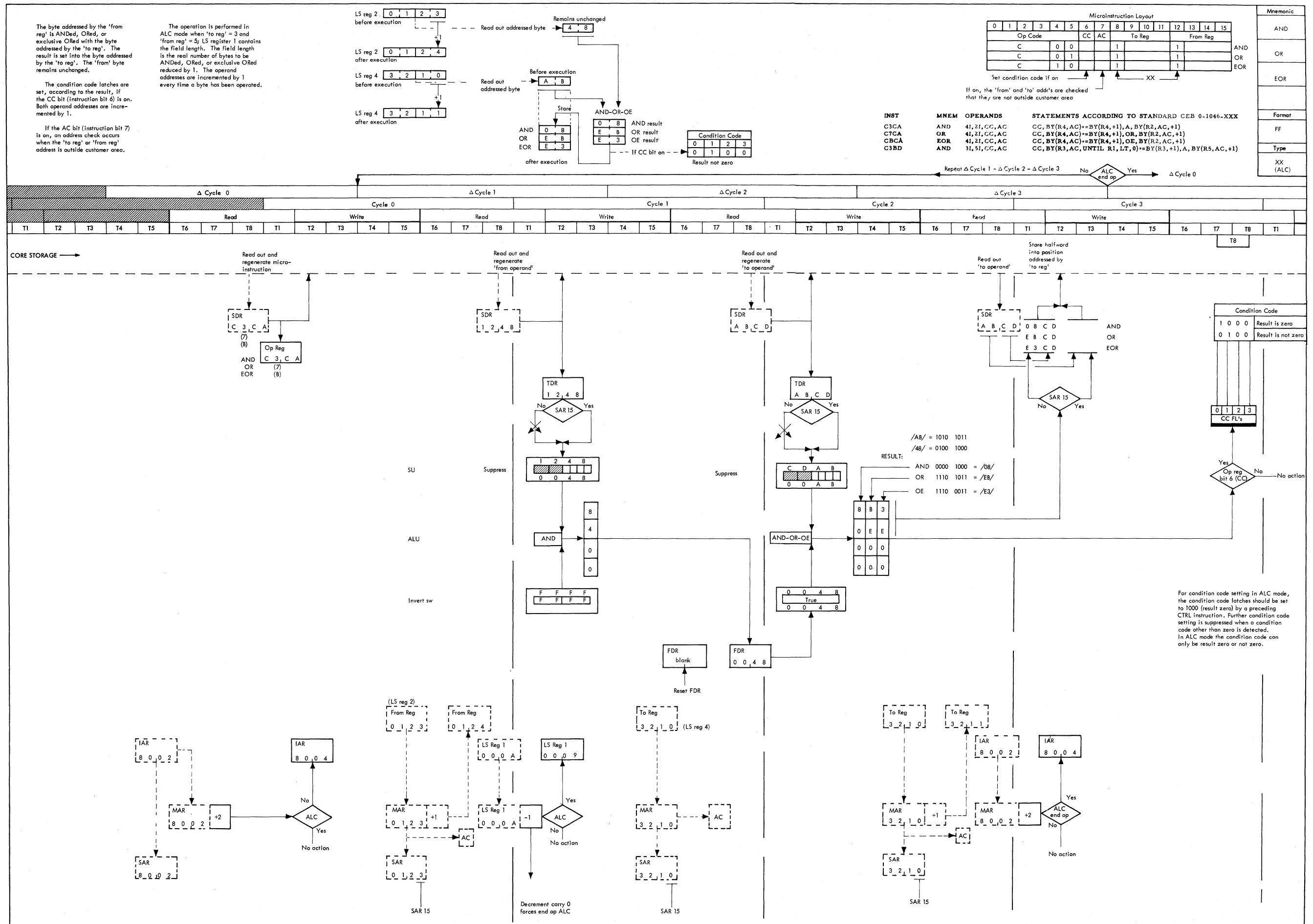


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

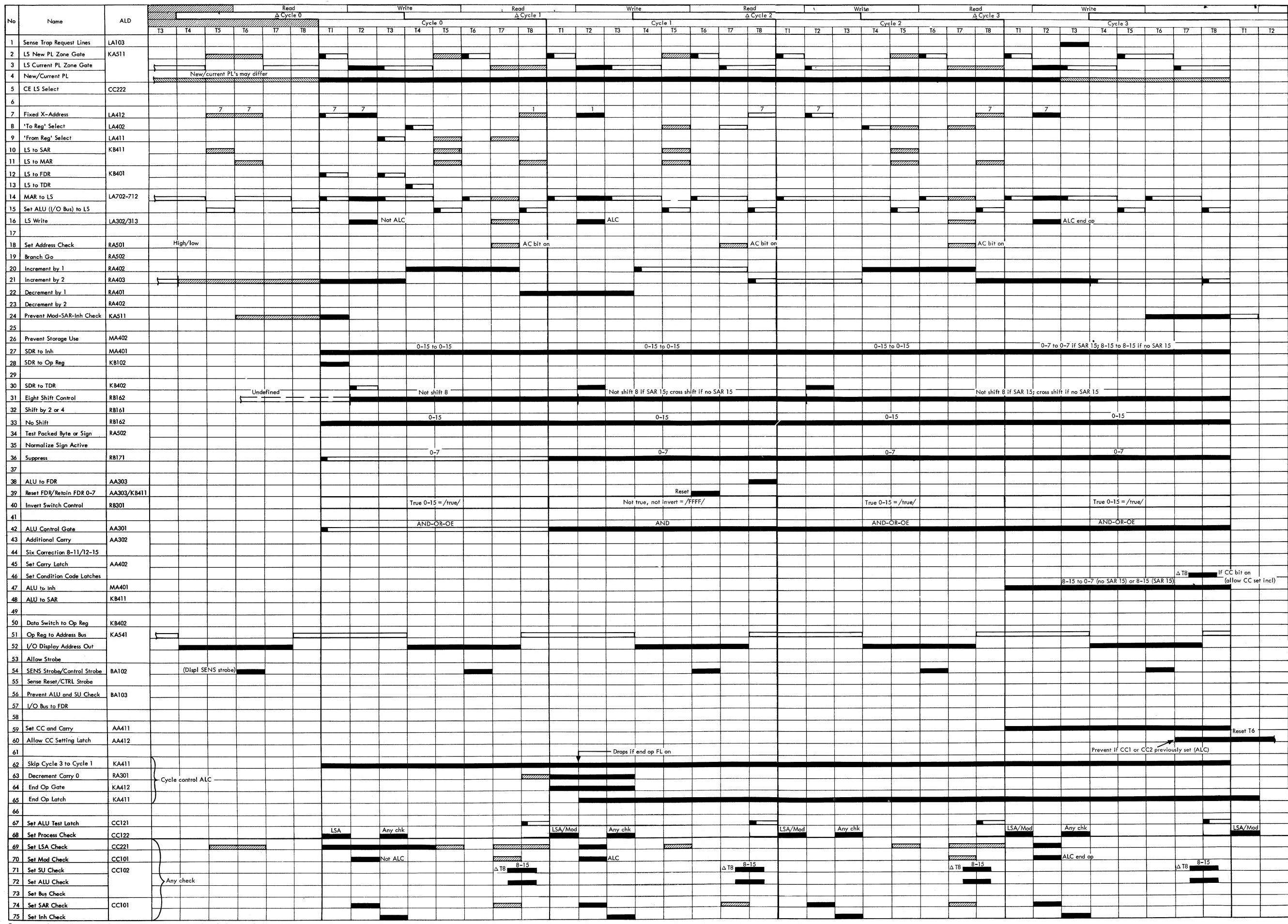


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

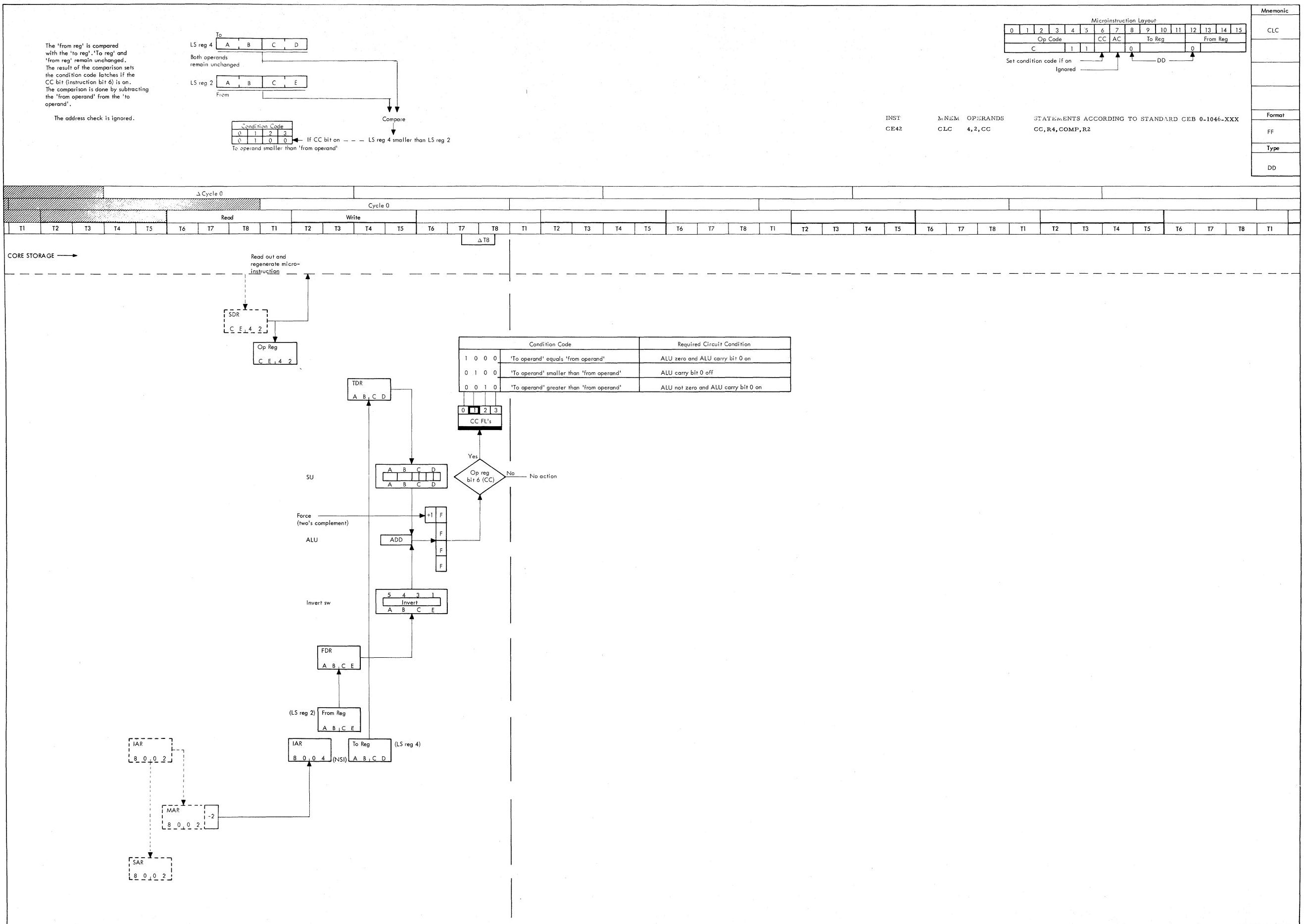


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

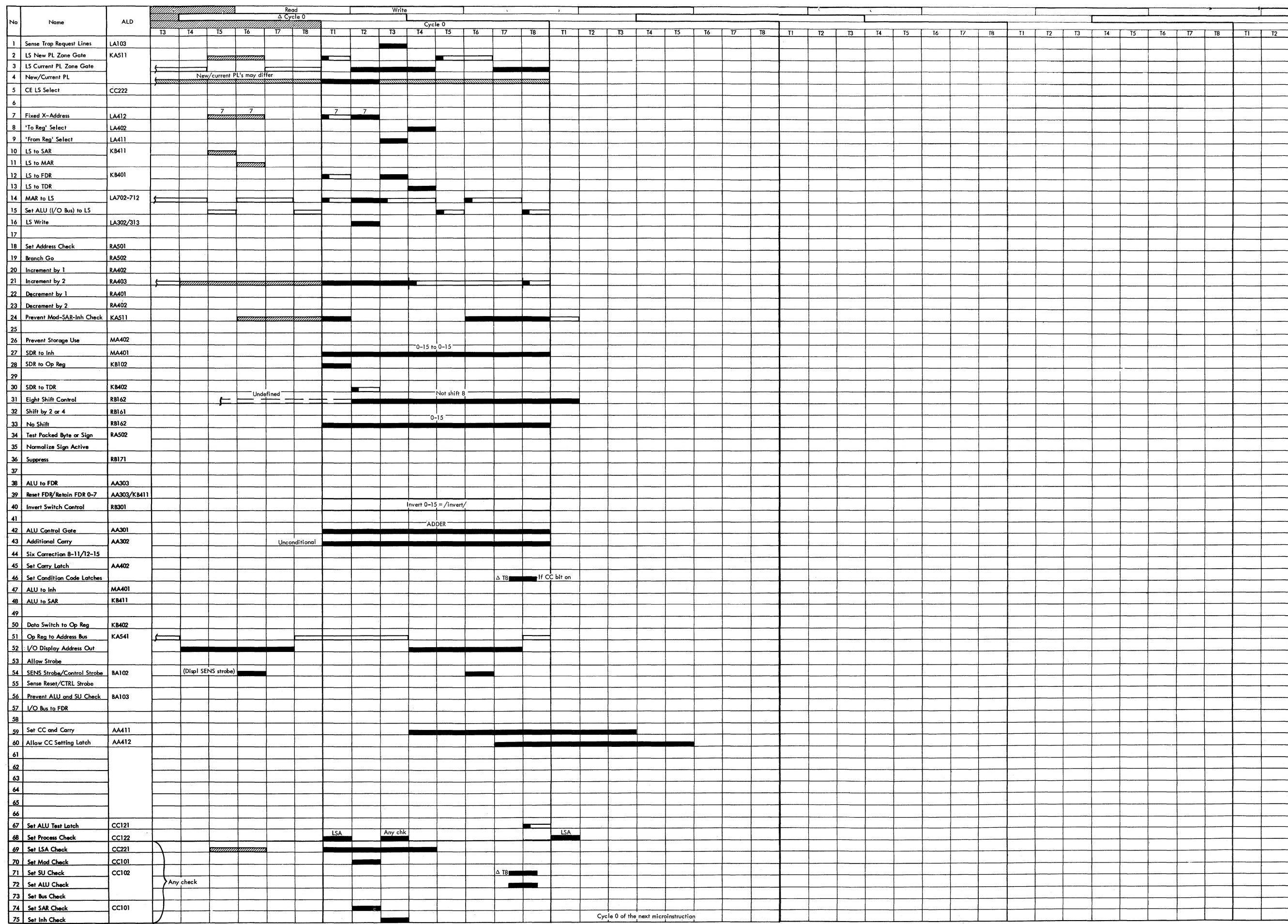
"Do not care" signals: ΔCycle Cycle



Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
 △Cycle (white box)
 Cycle (black box)

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

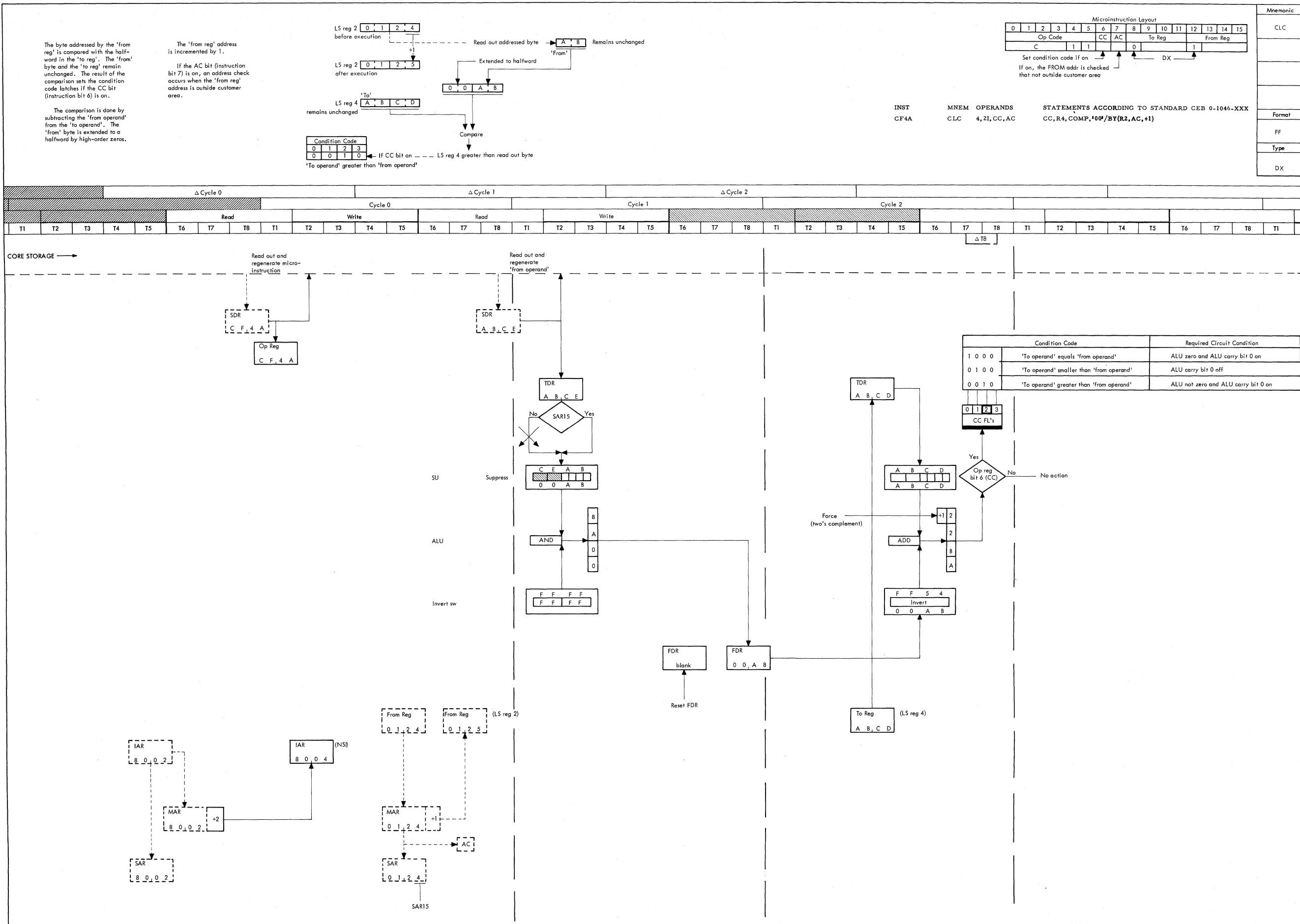


Function signals: ΔCycle Cycle "Do not care" signals: ΔCycle Cycle

"Do not care" signals: Δ Cycle Cycle

102755

10

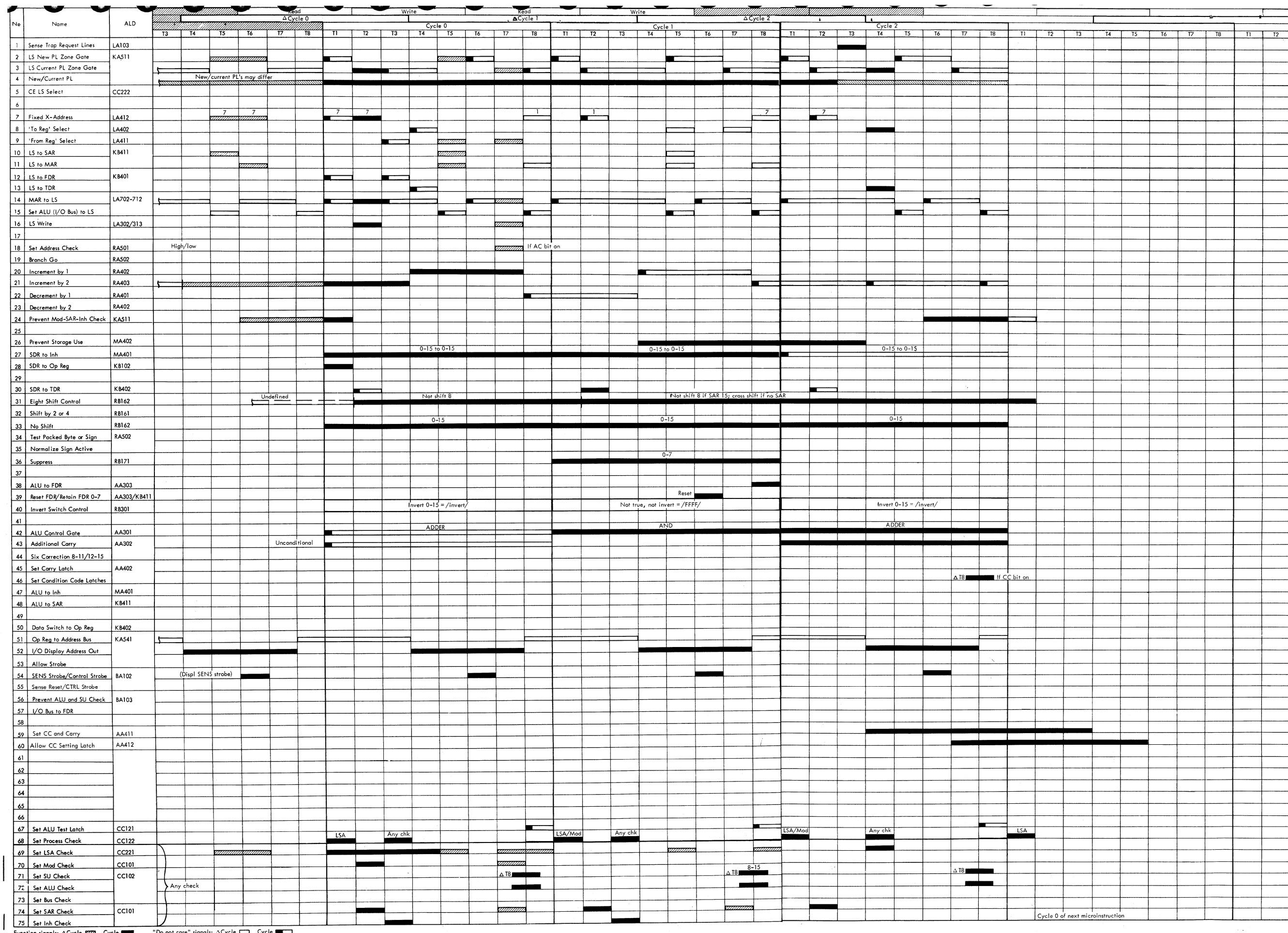


Mnemonic	CLC
Format	
FF	
Type	
DX	

Note: For "Do not care" functions refer to timing chart below.

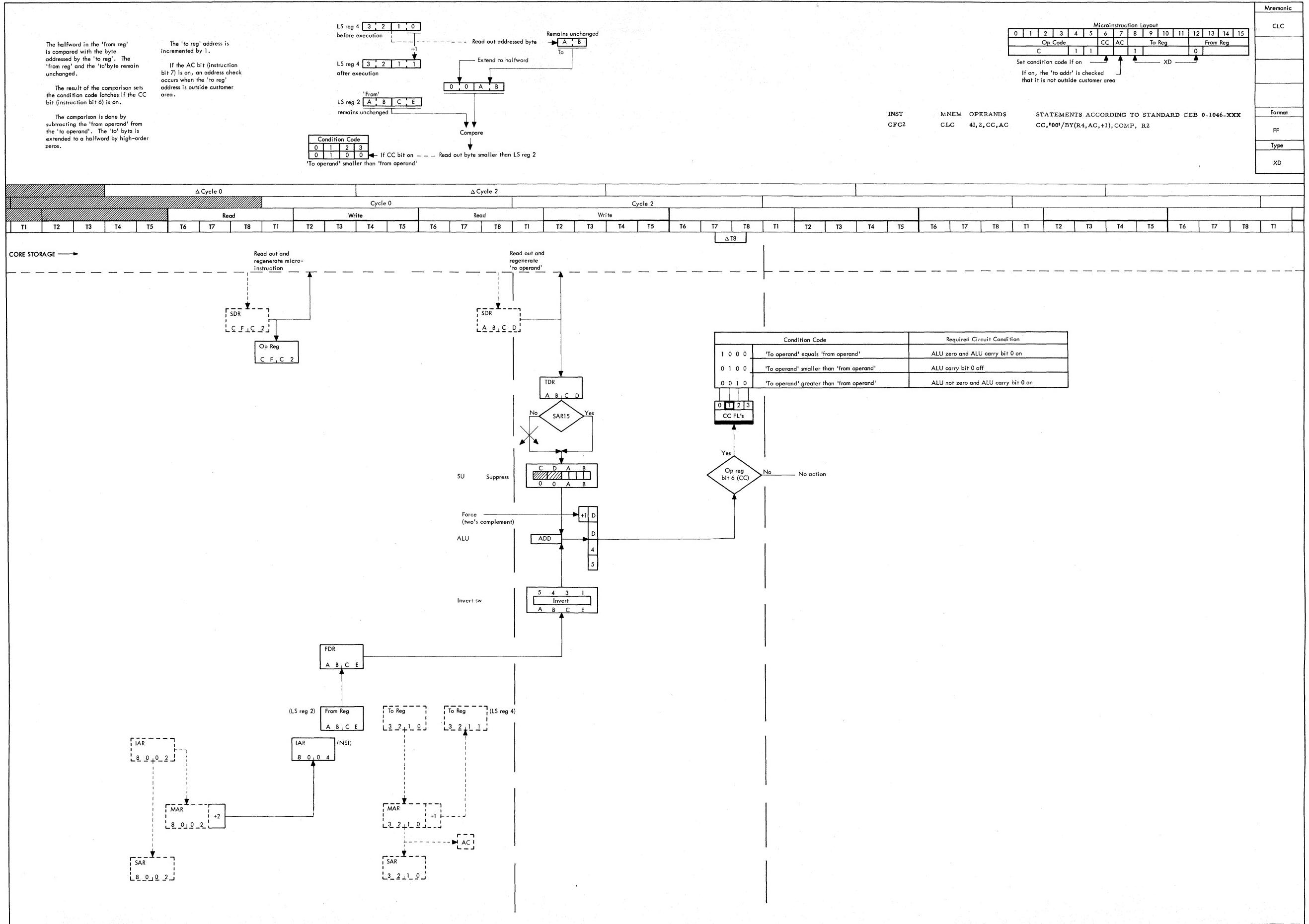
"Do not care" signals:
 ΔCycle []
 Cycle []

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

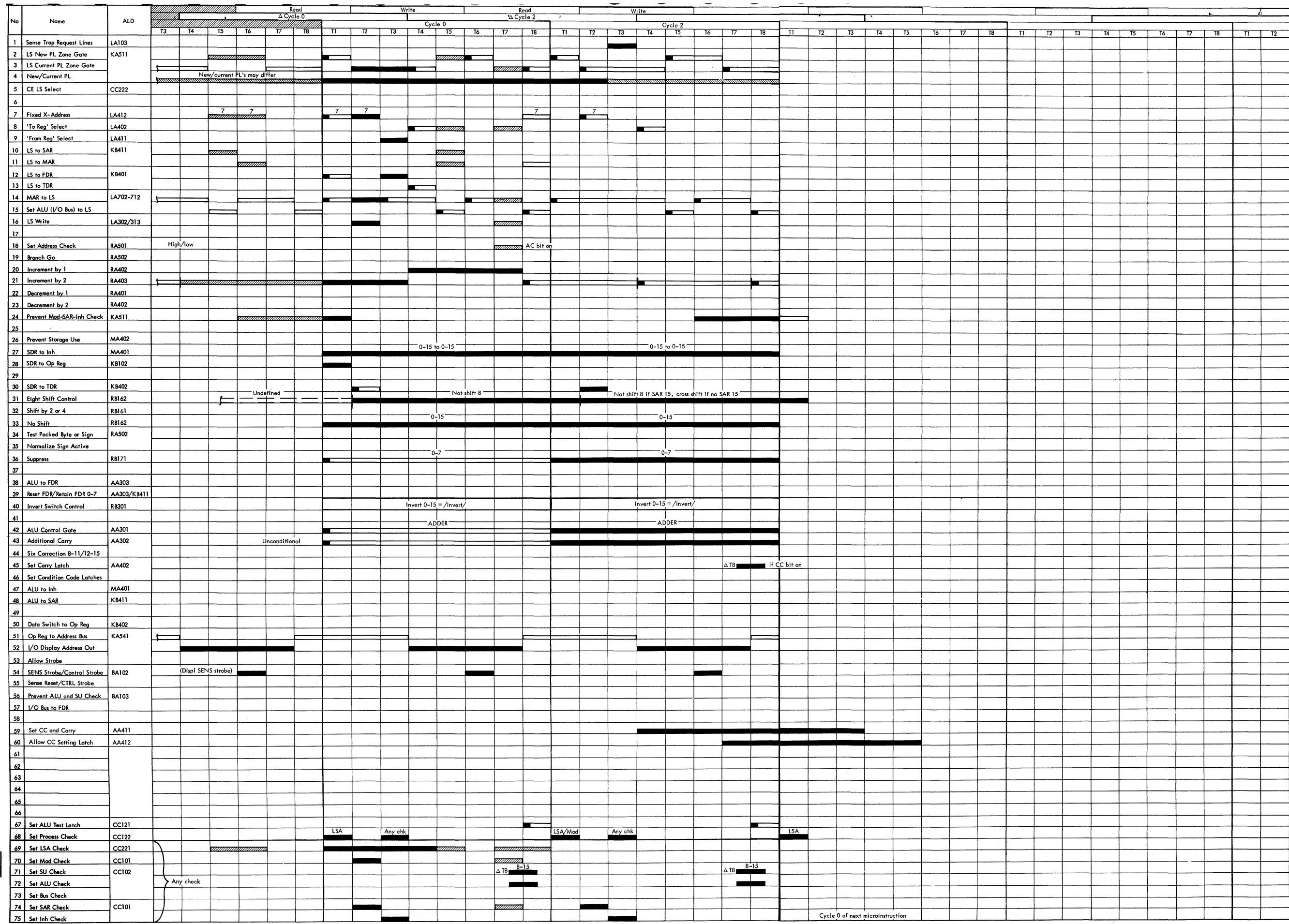


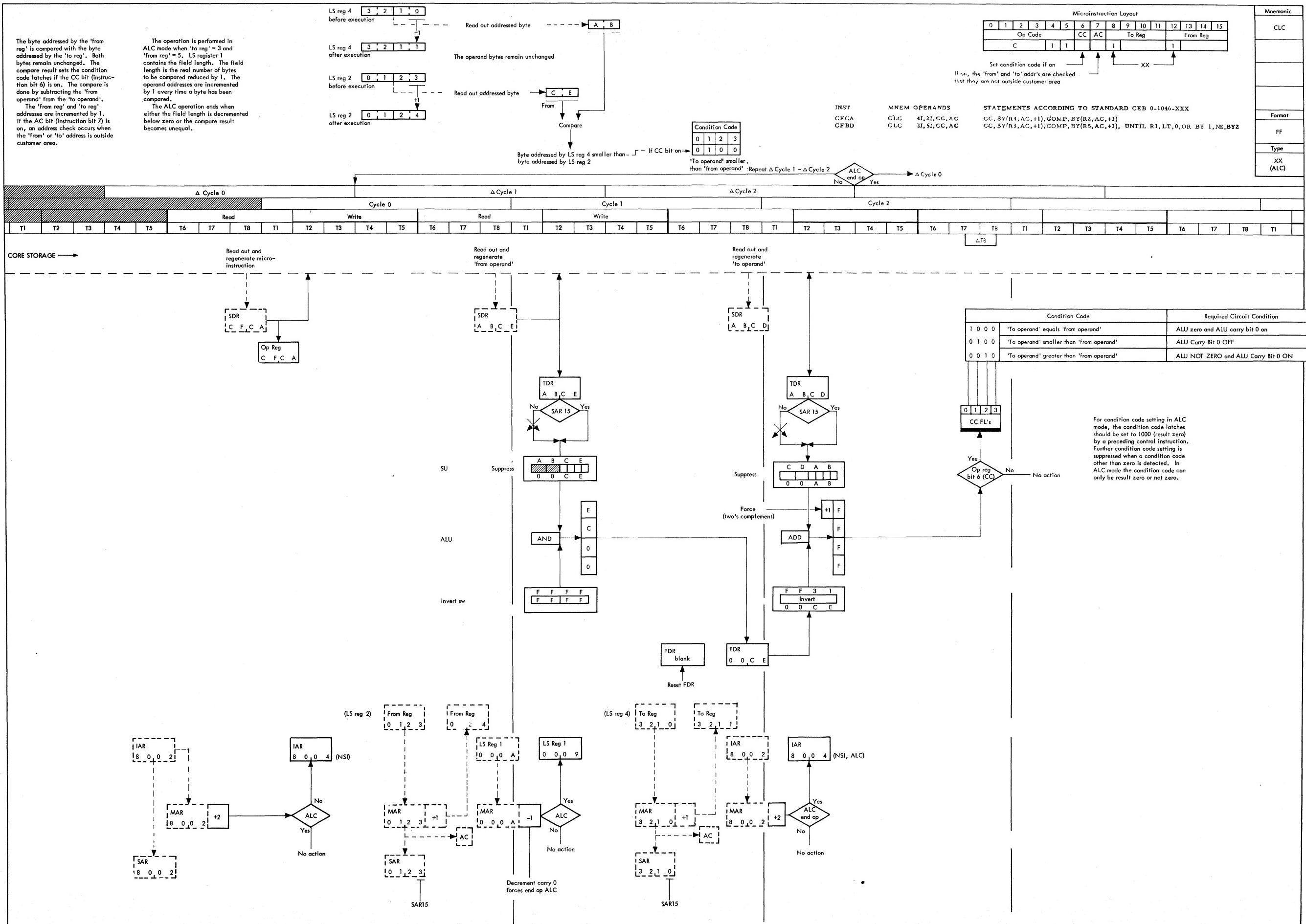
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle .Cycle

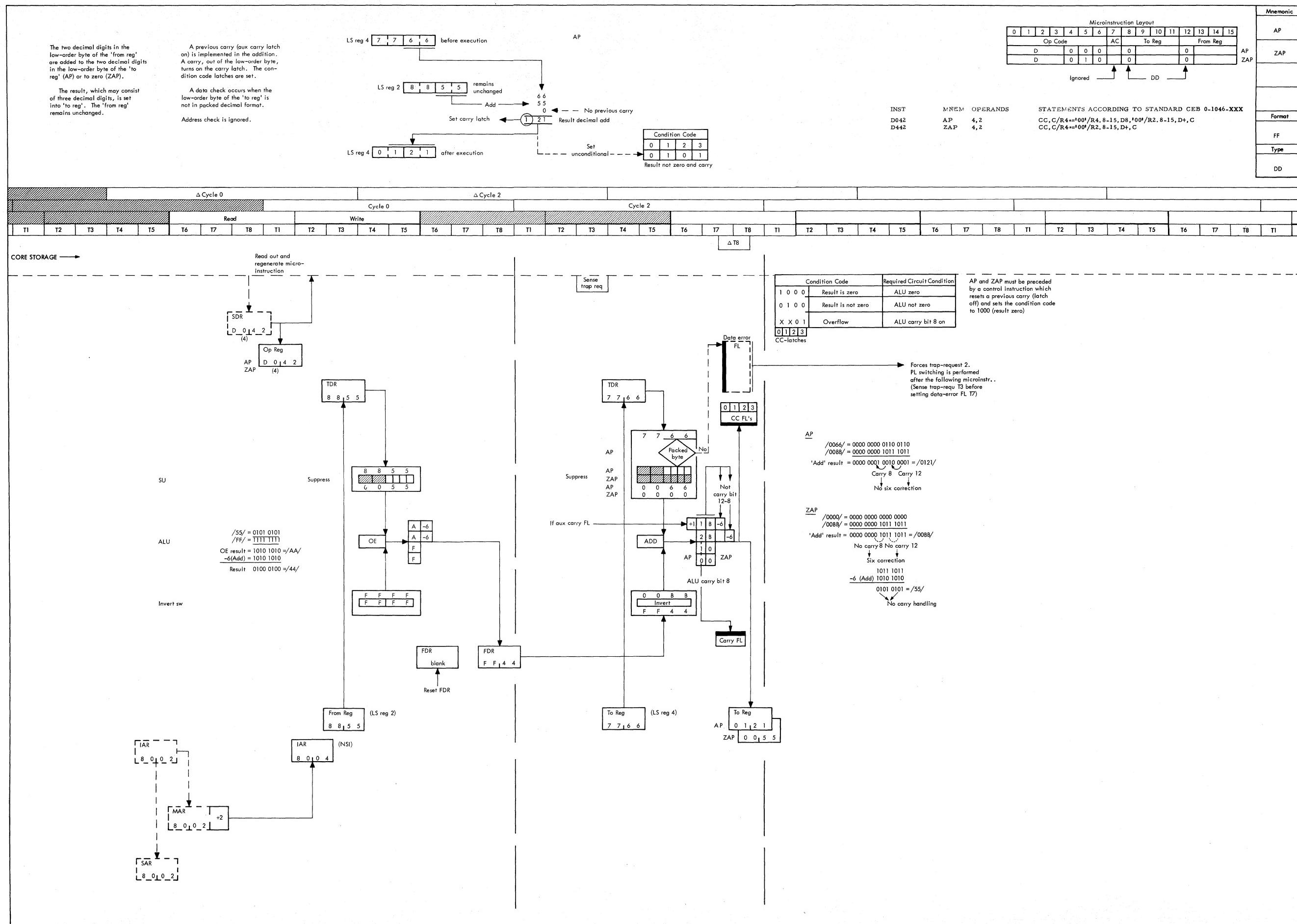
"Do not care" signals: Δ Cycle .Cycle



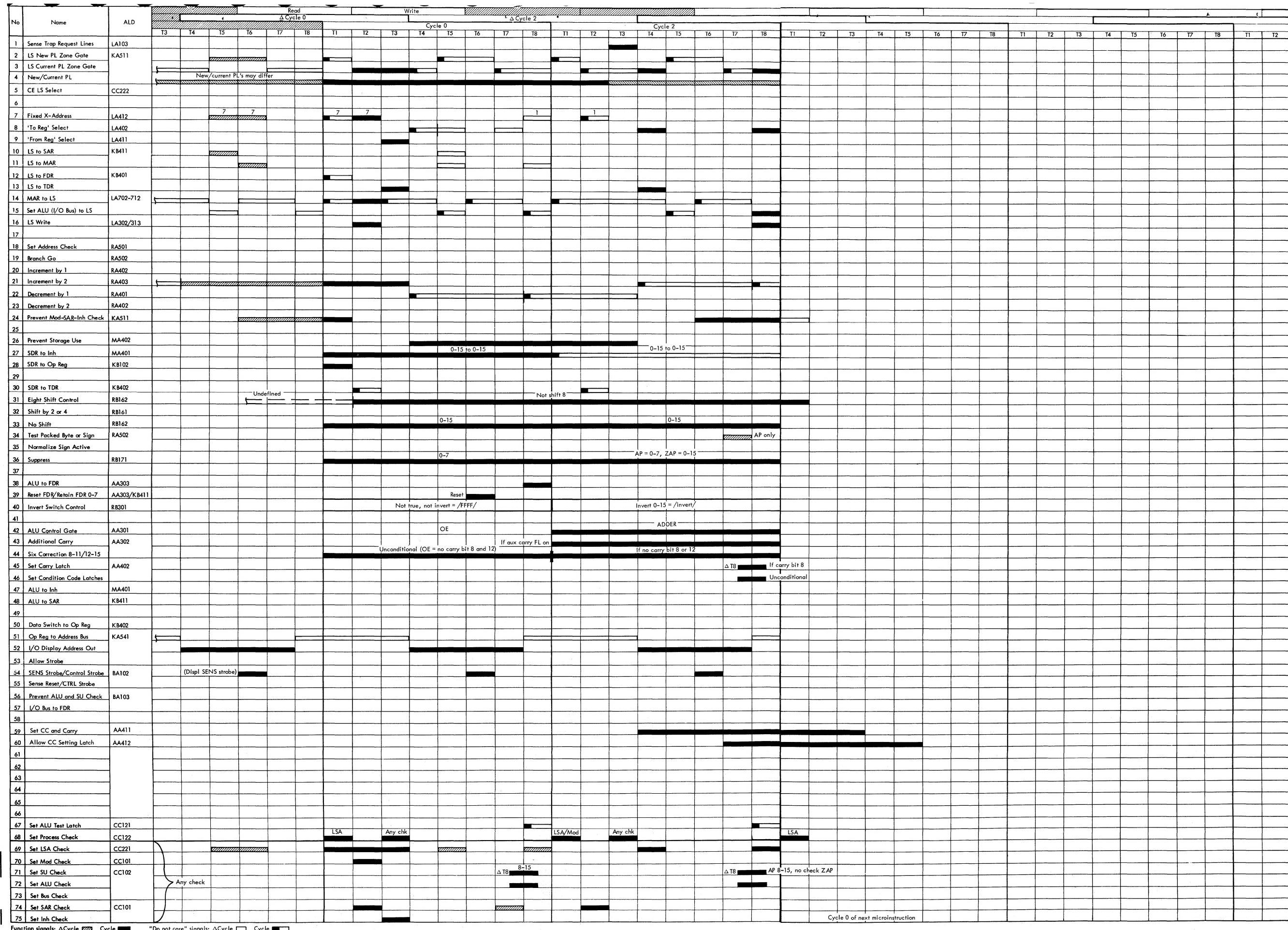
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.







Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

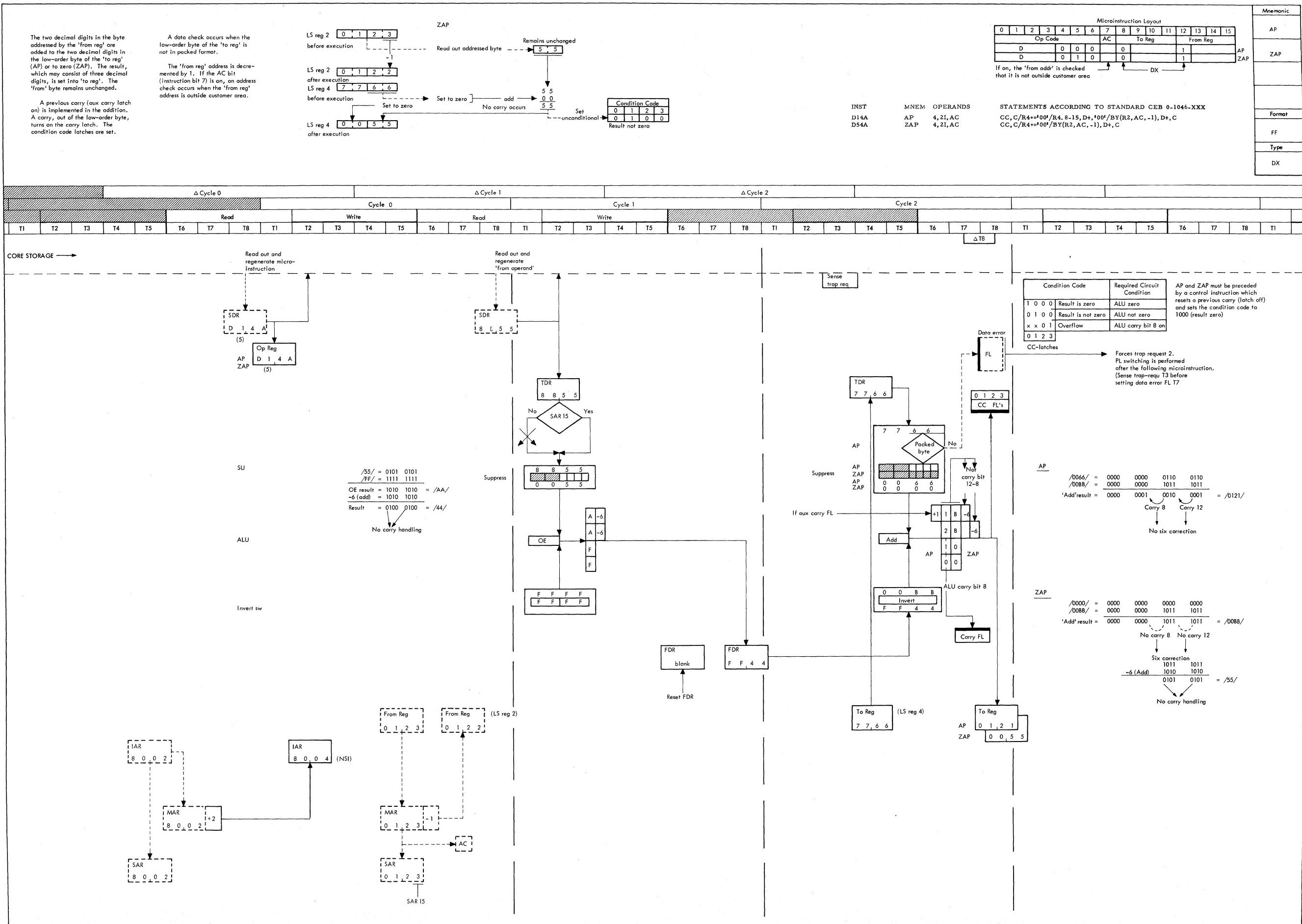


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

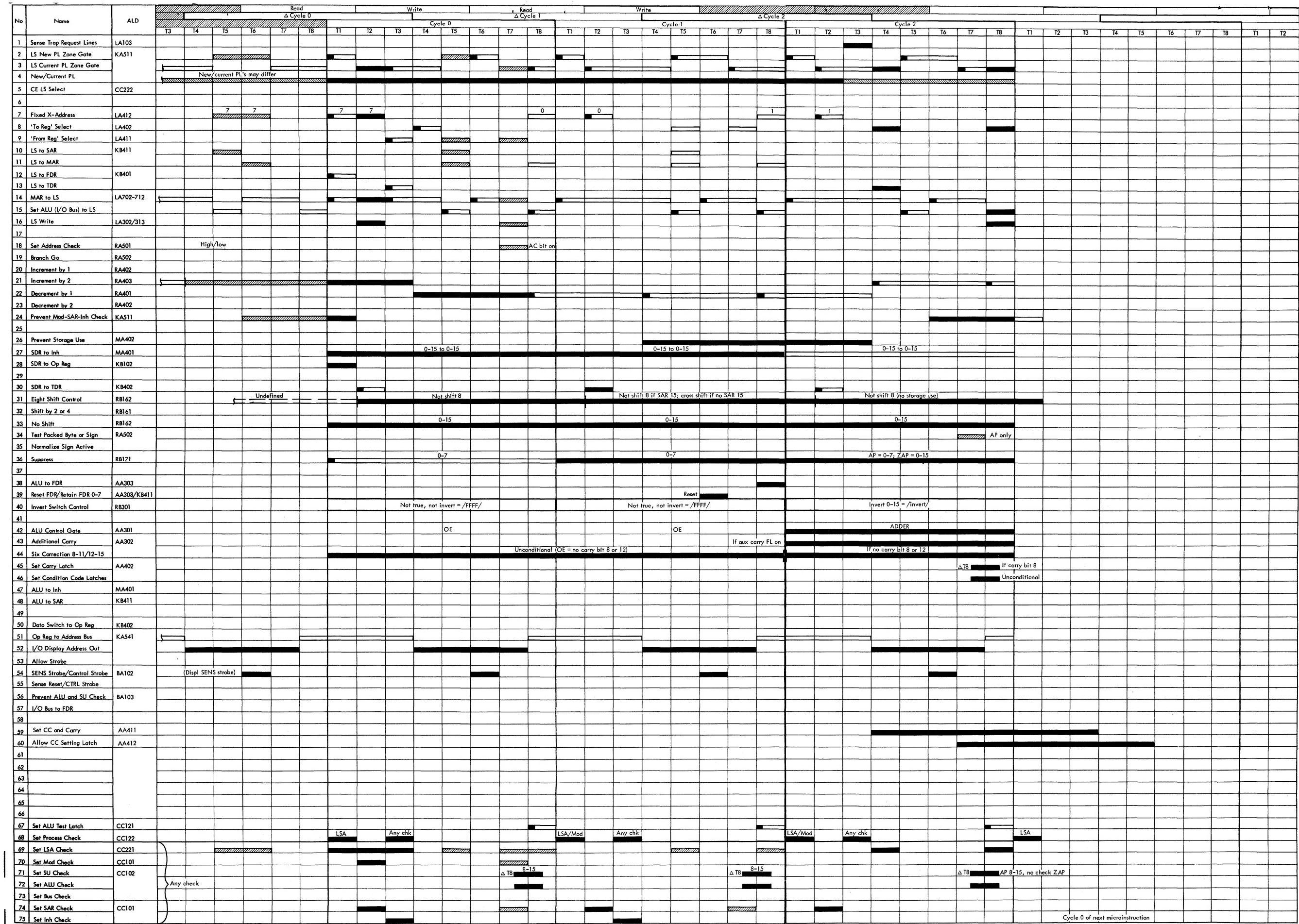
(03759A)

2020 >

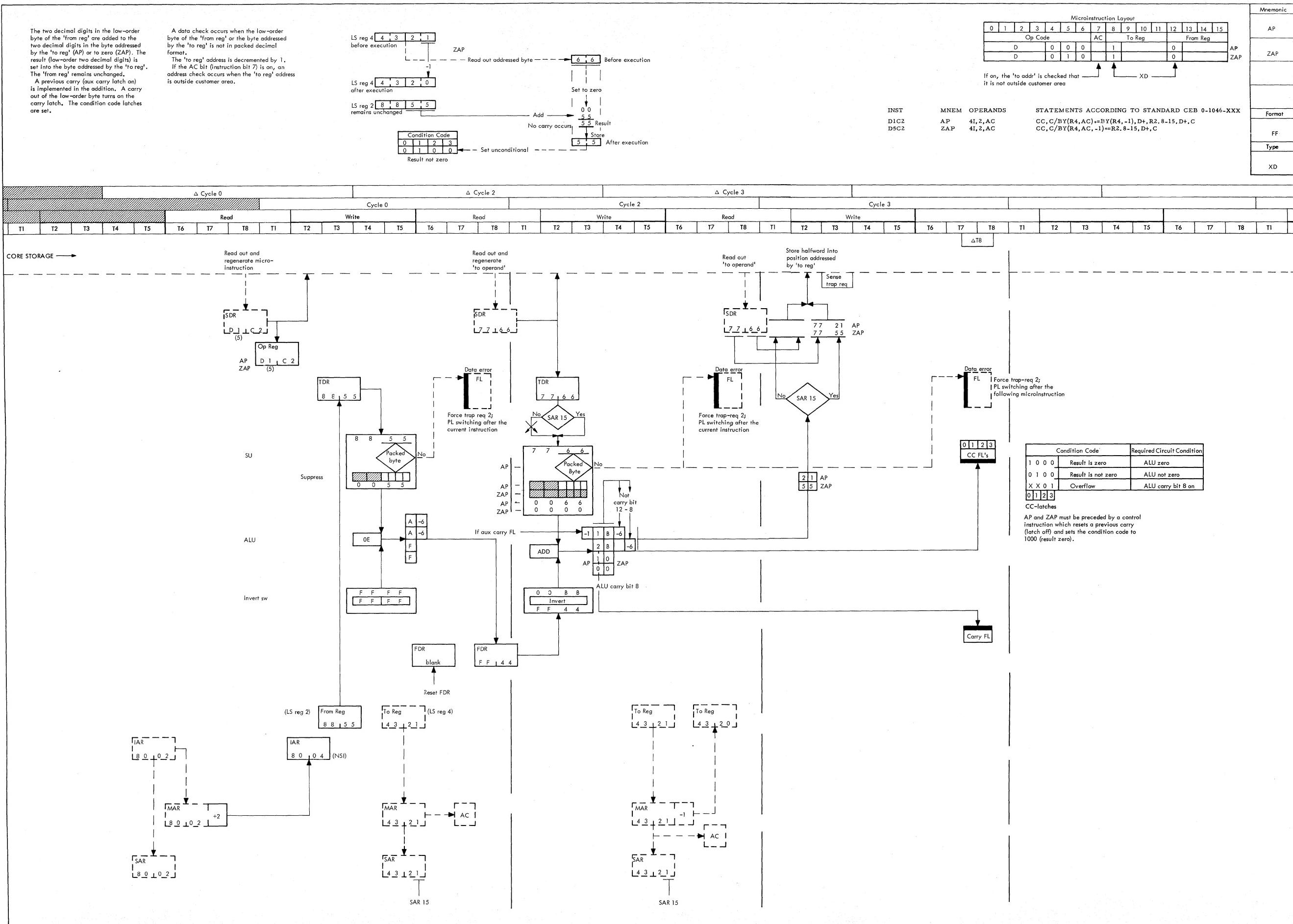
50 000 EFMDD Vol 2 (8/69)



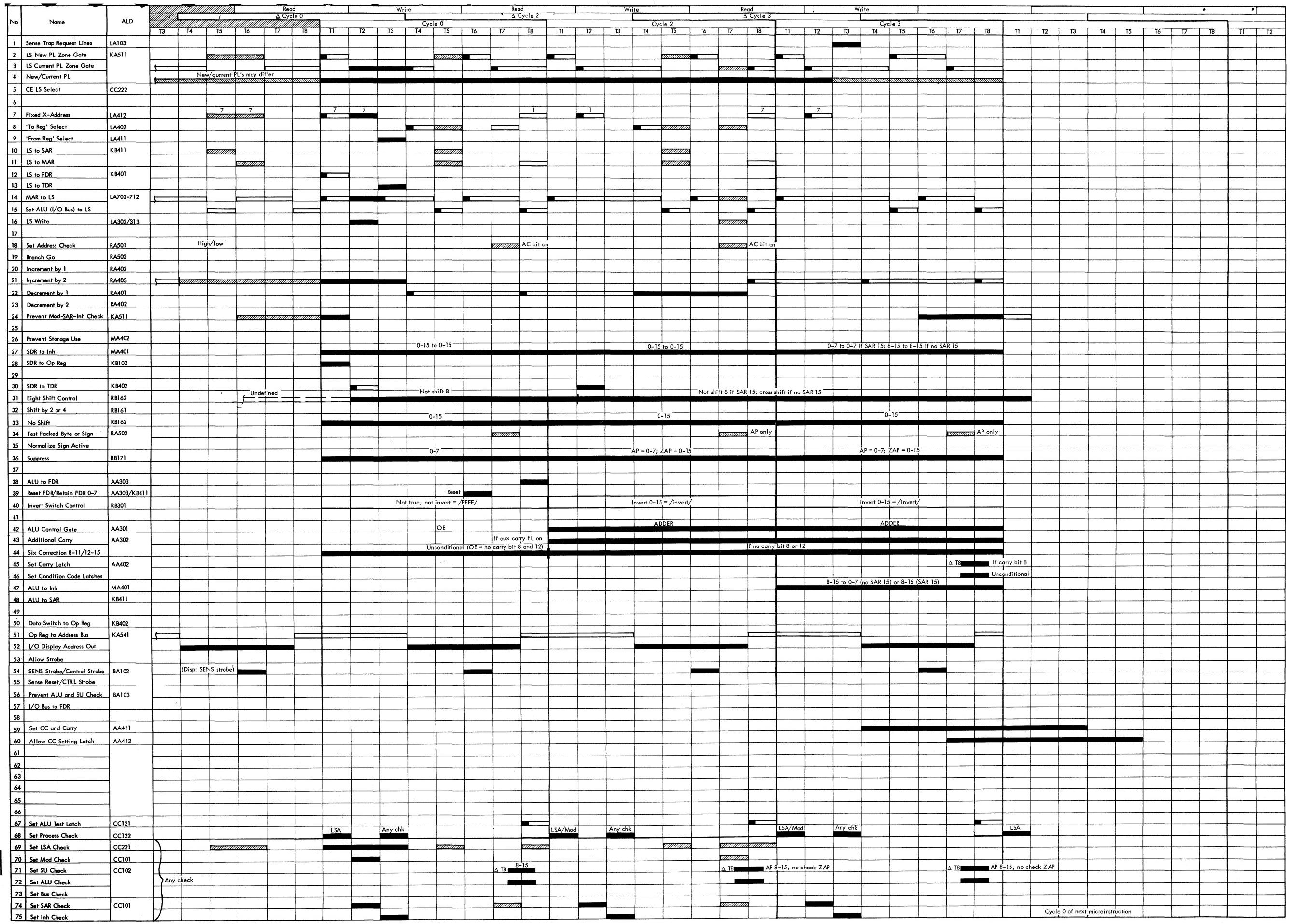
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: □ Cycle ■ □ "Do not care" signals: □ Cycle ■ □ Cycle ■

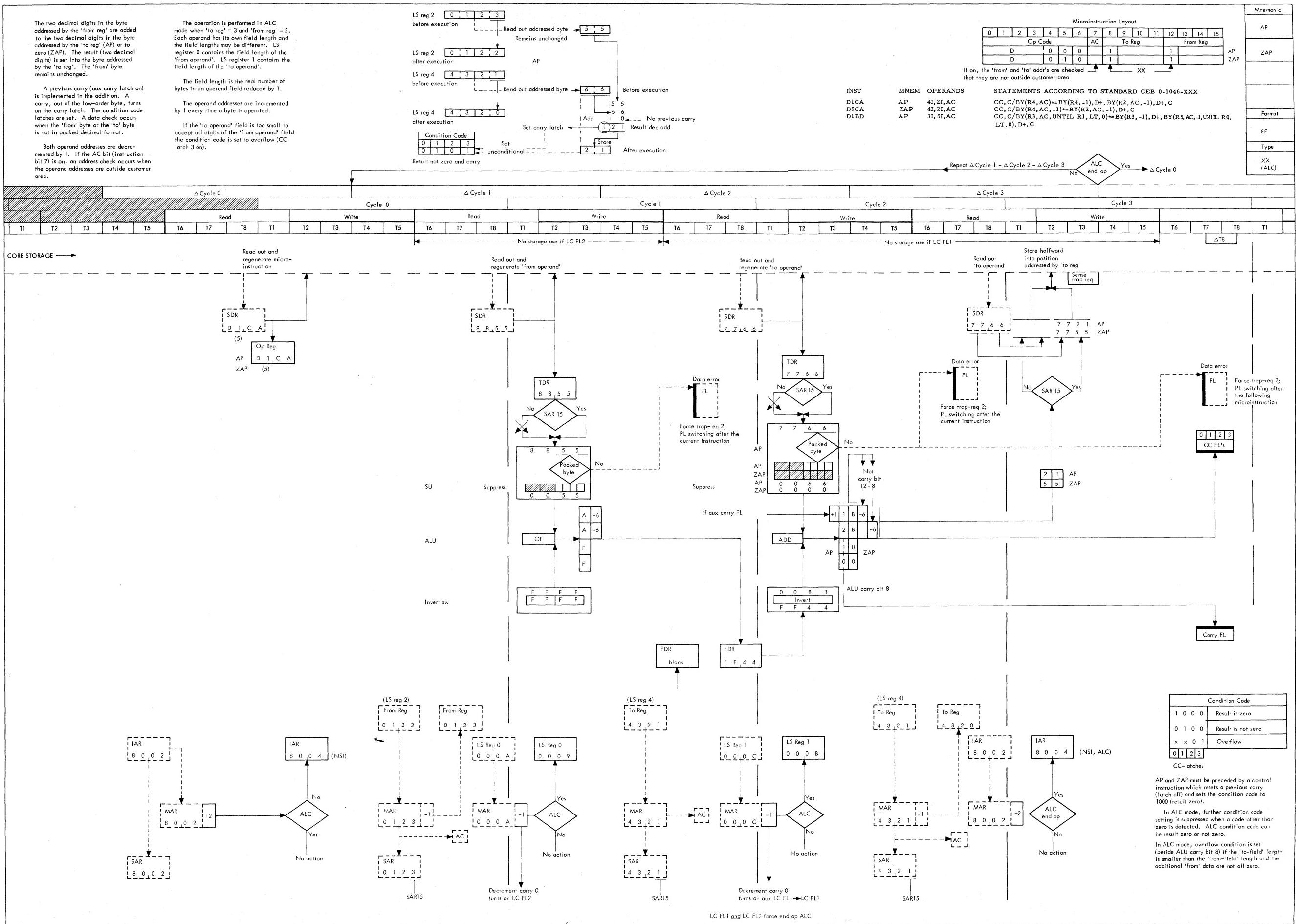


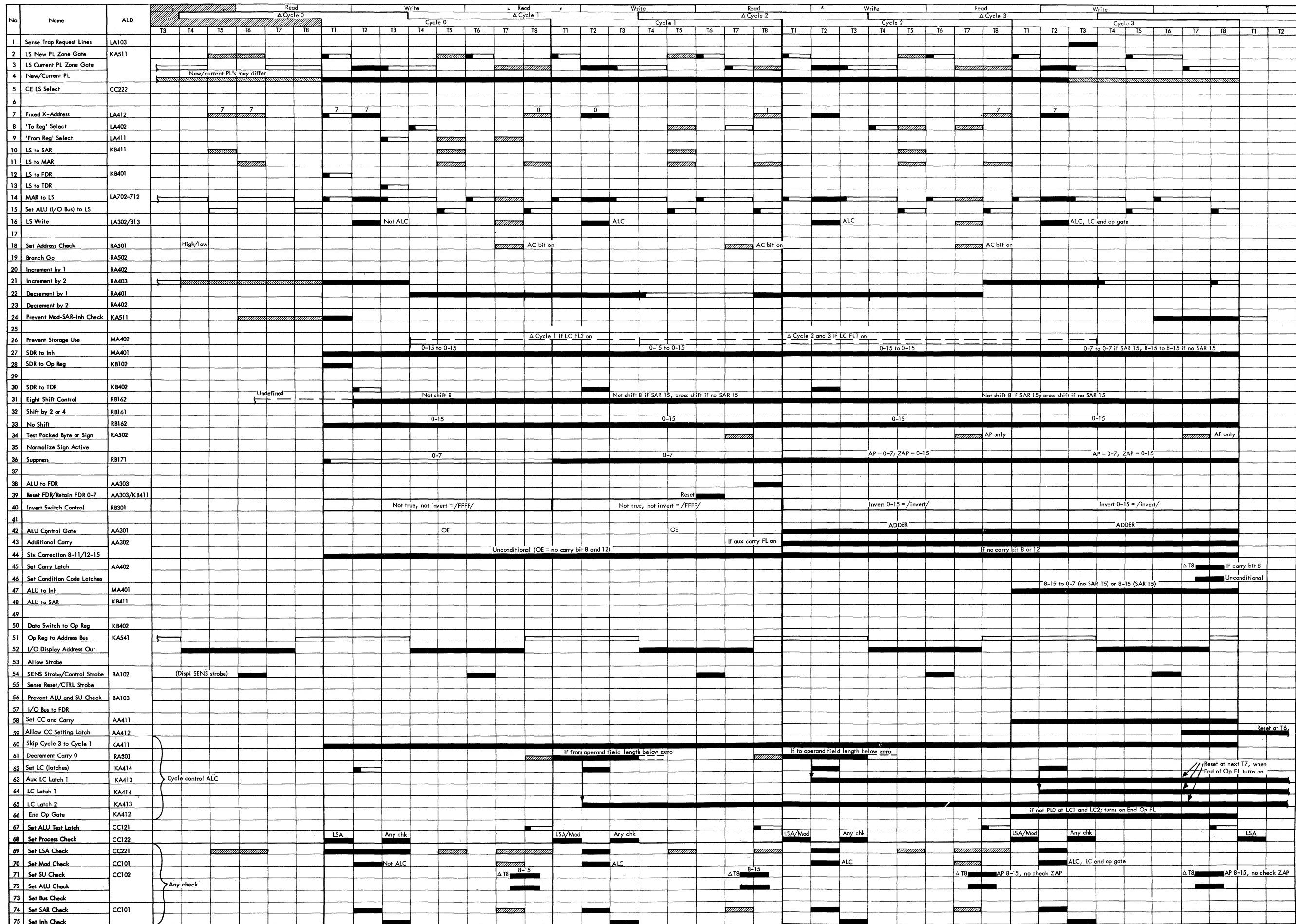
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

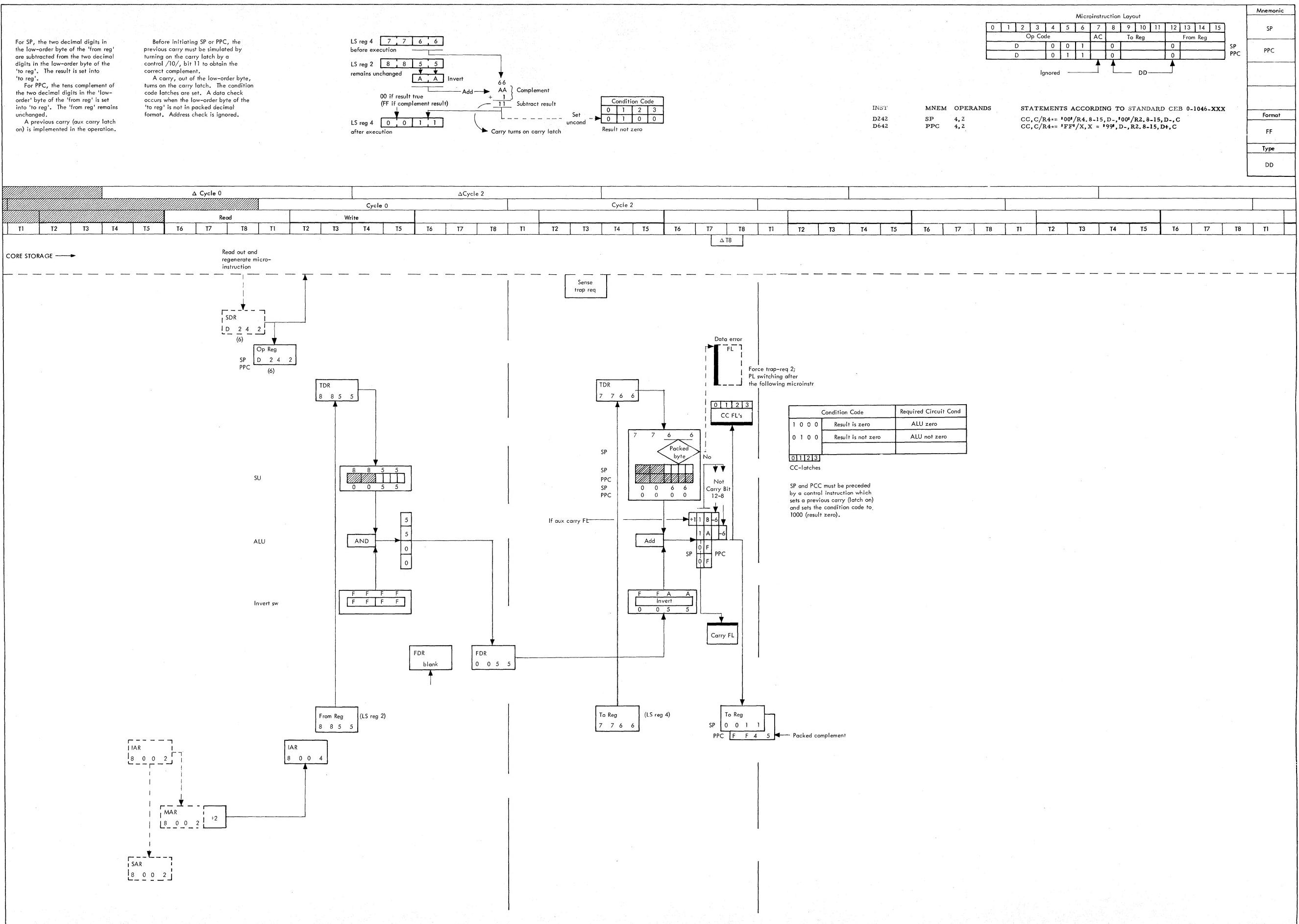


Function signals: ΔCycle Cycle "Do not care" signals: ΔCycle Cycle

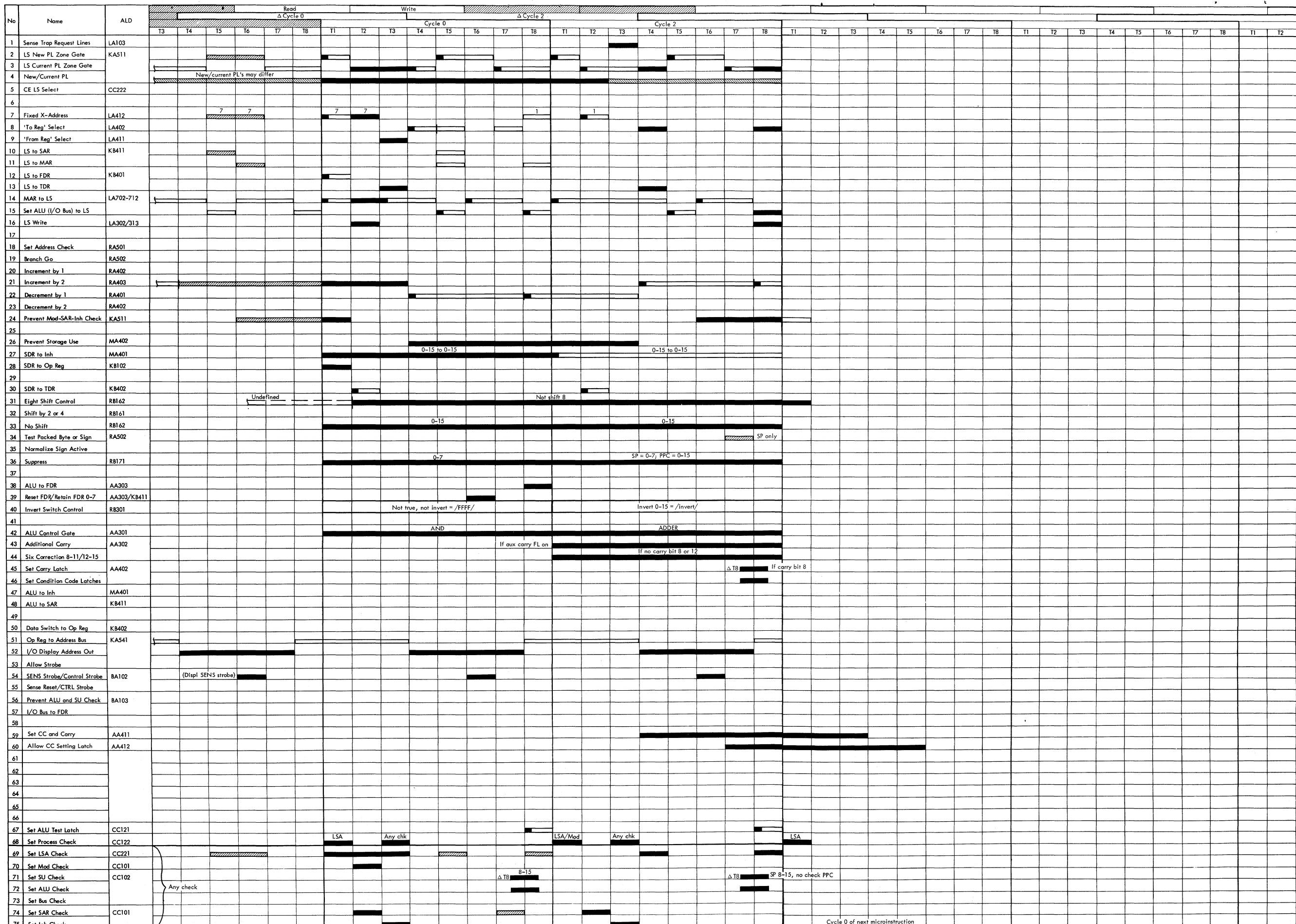
"Do not care" signals: Δ Cycle Cycle





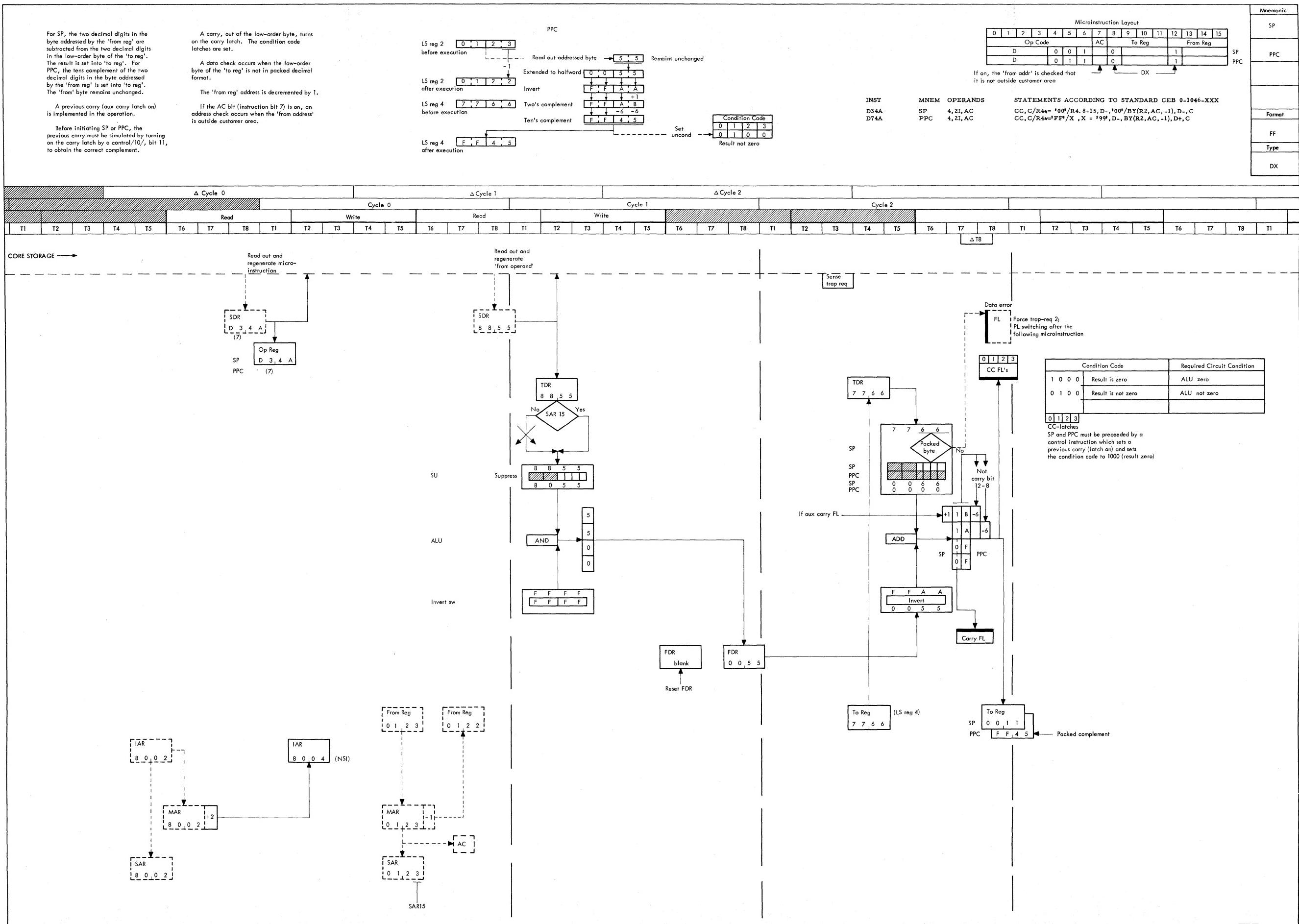


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

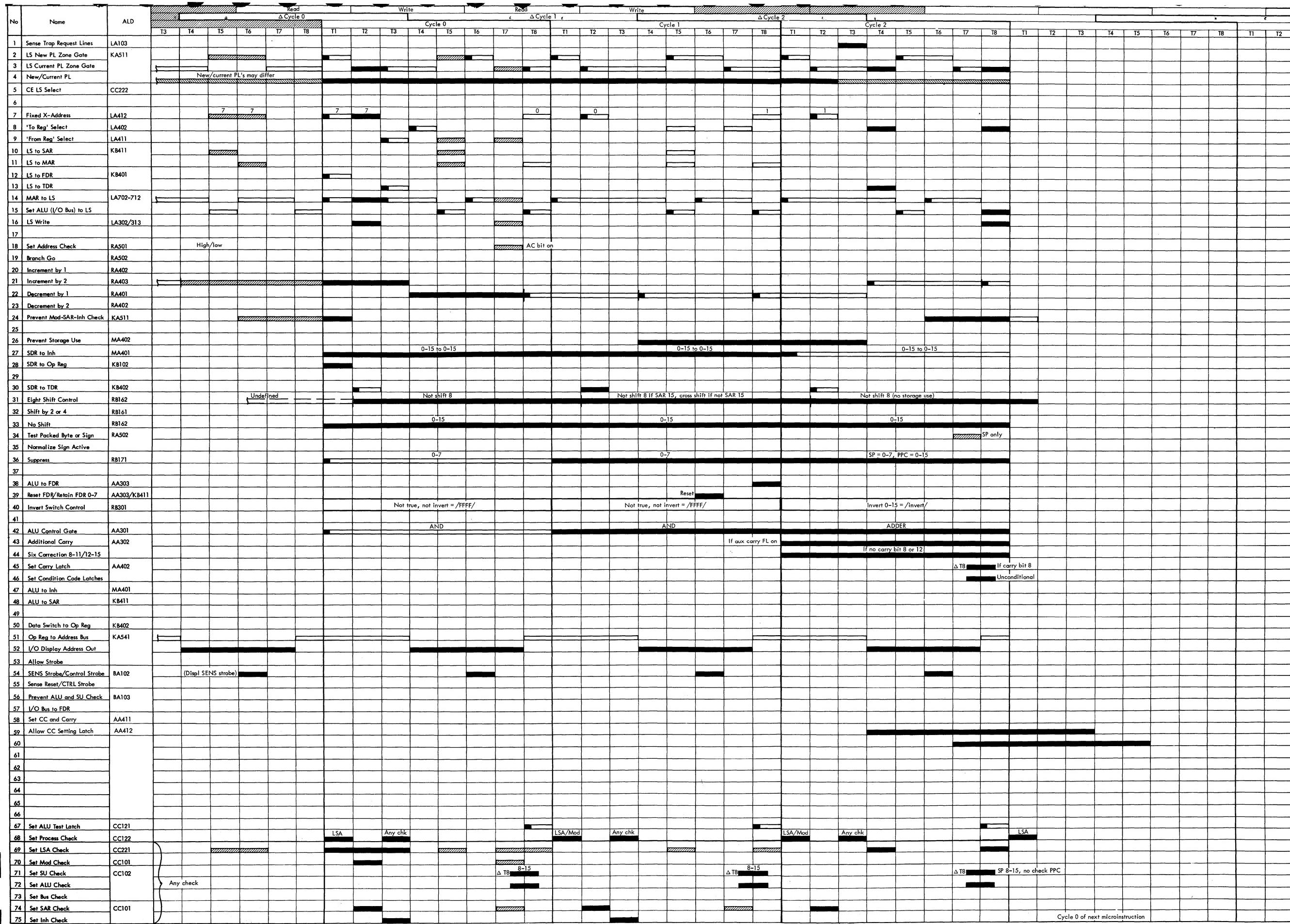
"Do not care" signals: Δ Cycle Cycle

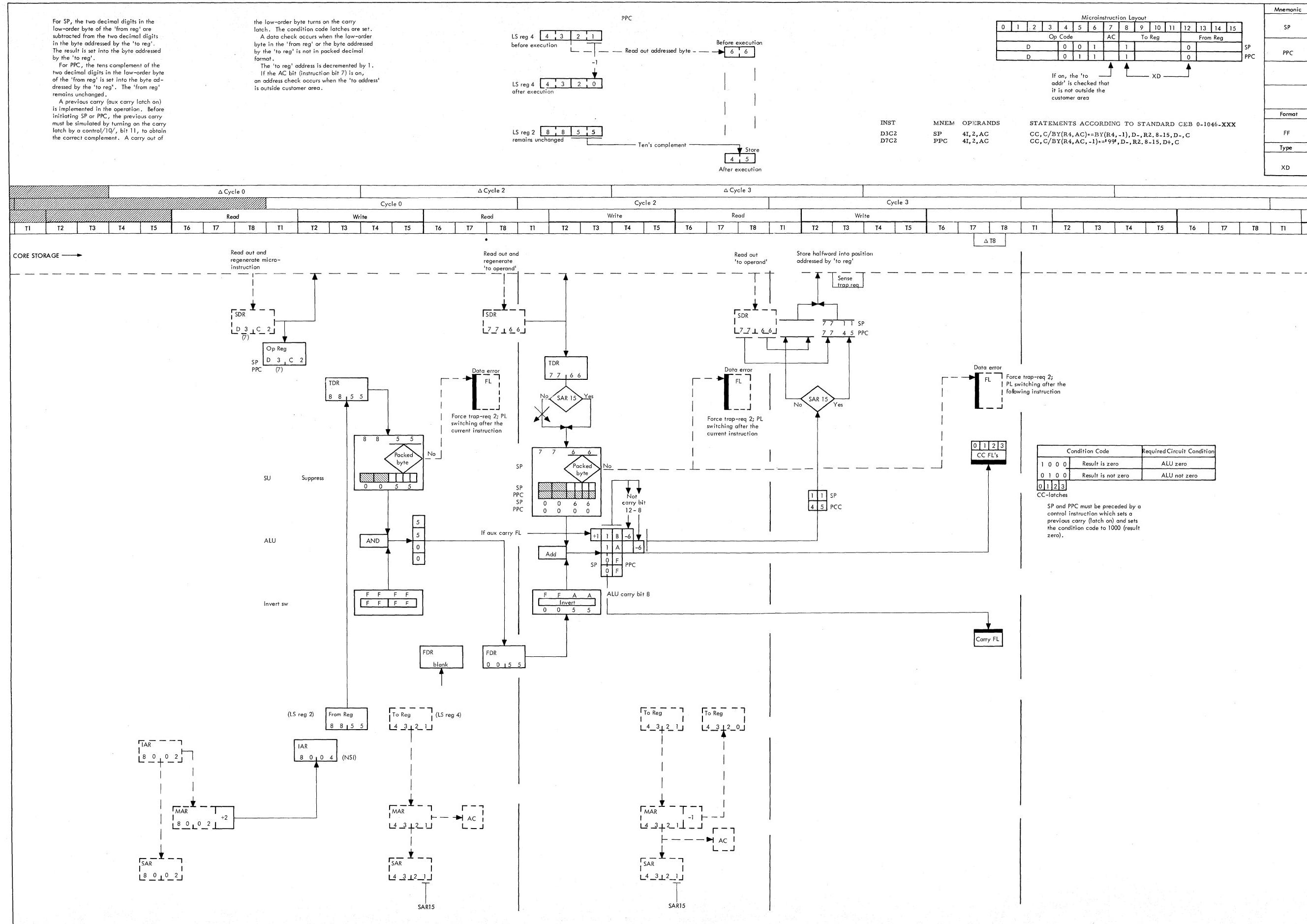


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

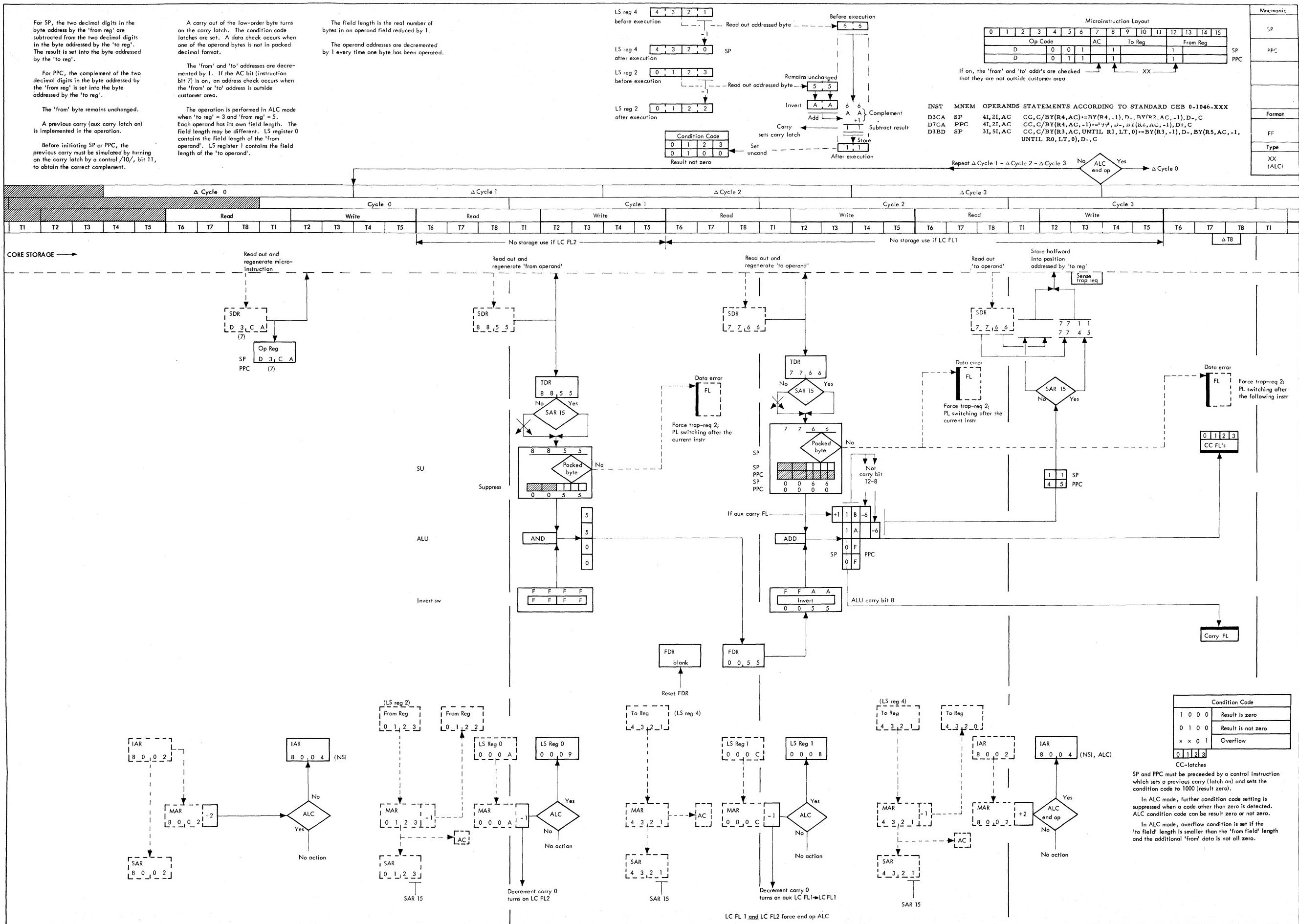
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
 ΔCycle
 Cycle





Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

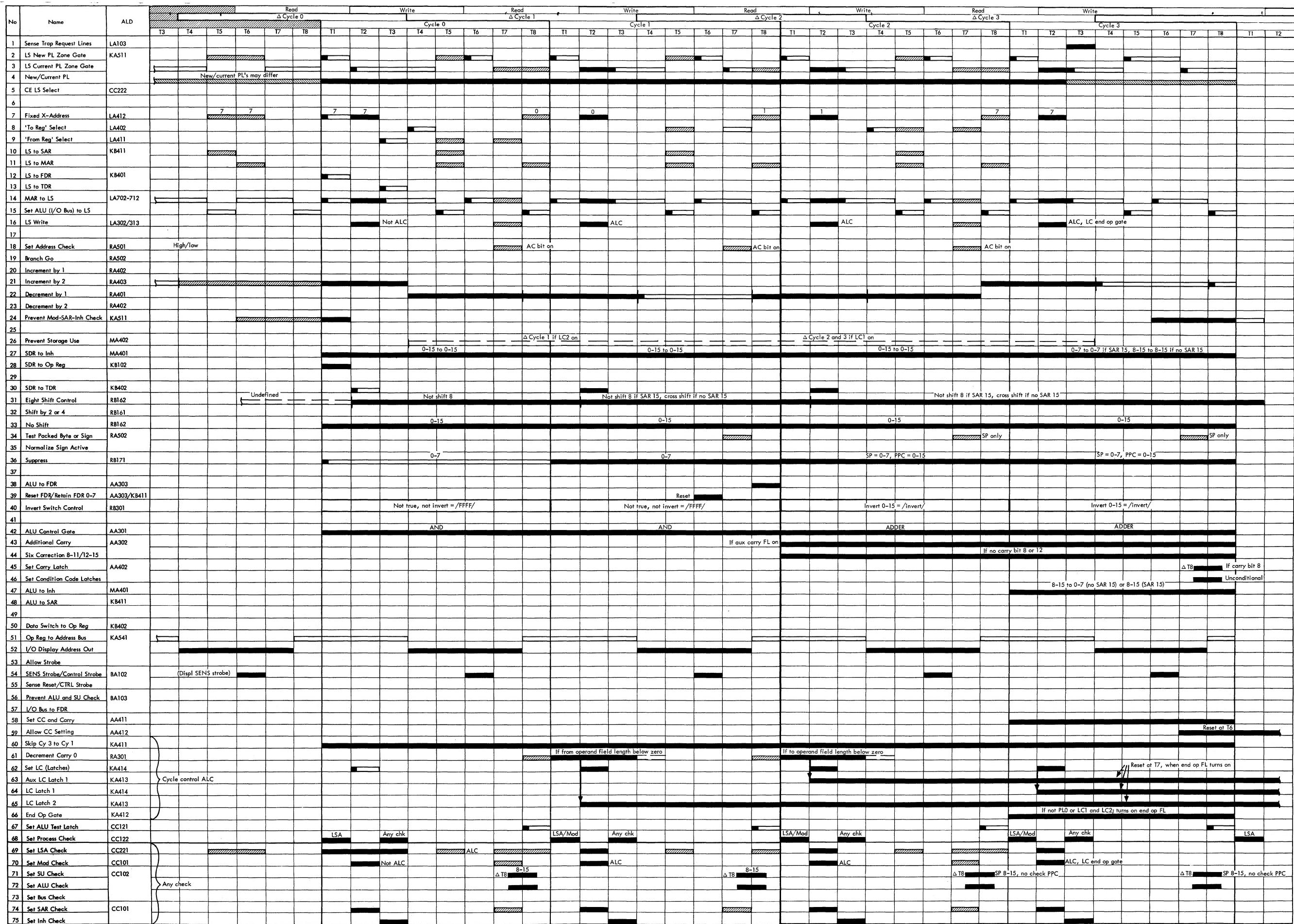


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-61. Subtract Packed Byte/Perform Packed Complement (XX, ALC) (Part 1 of 2)

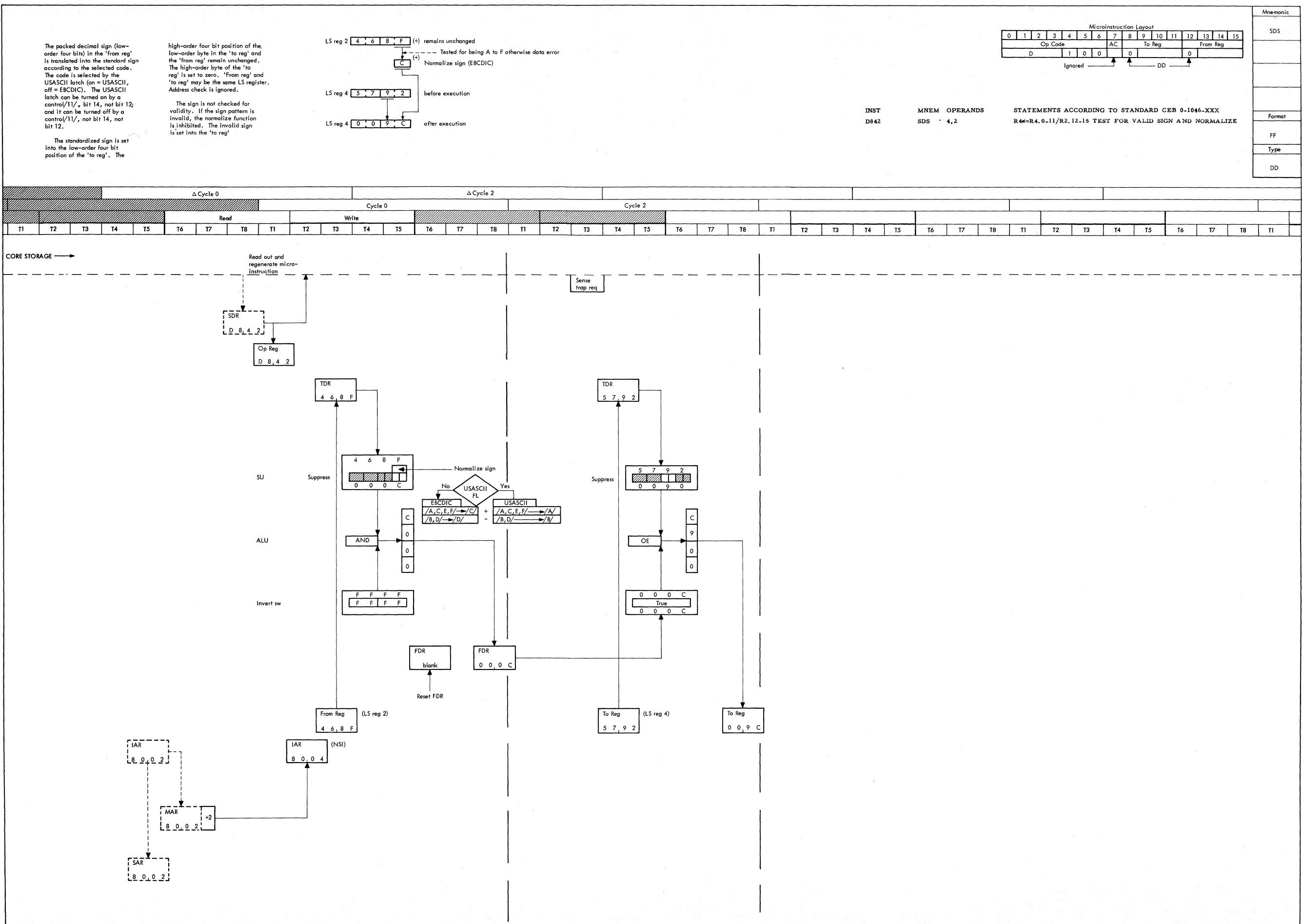
(03766)

2020 ≥ 50,000 FEMDM Vol 2 (8/69)



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

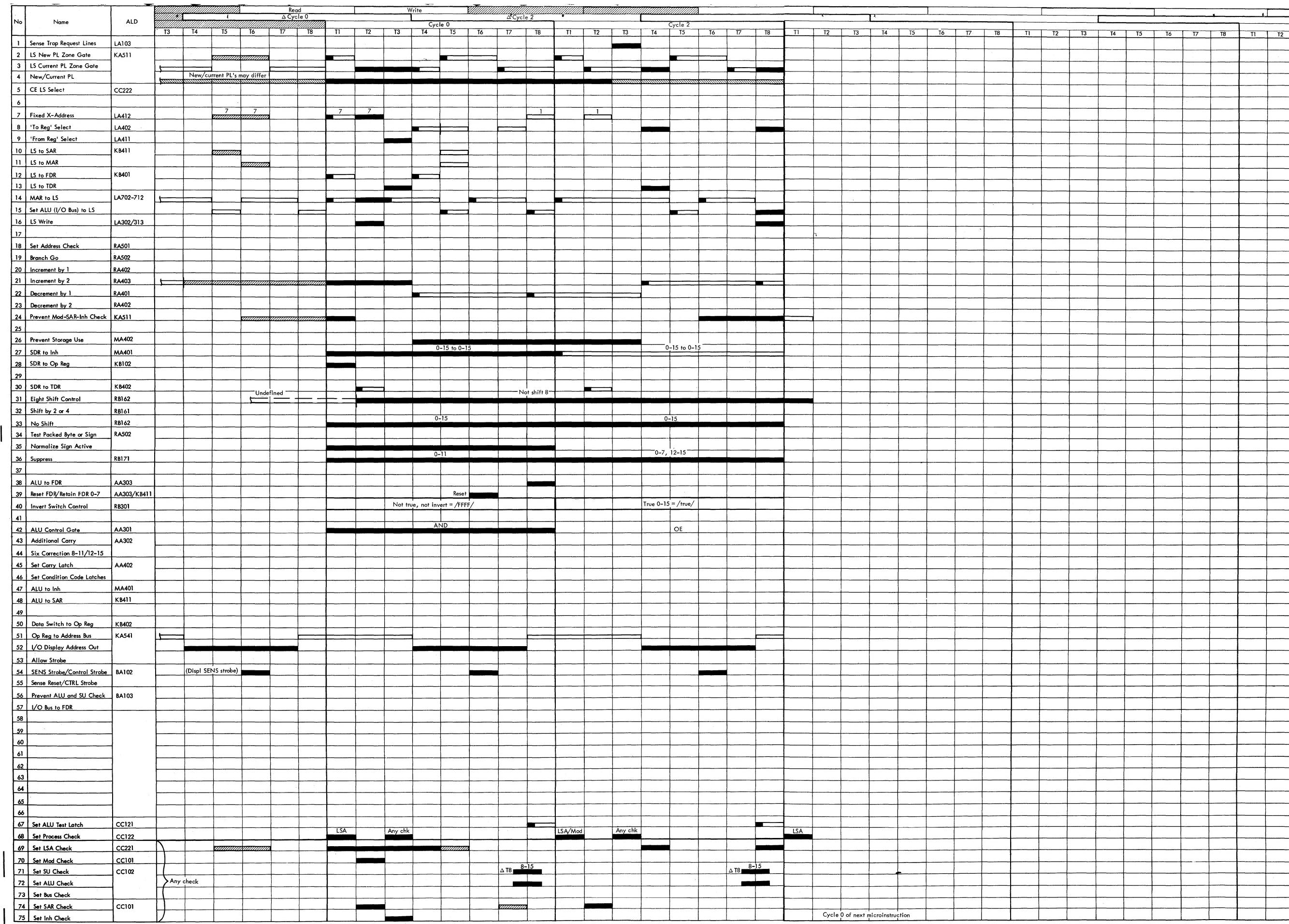
"Do not care" signals: Δ Cycle Cycle

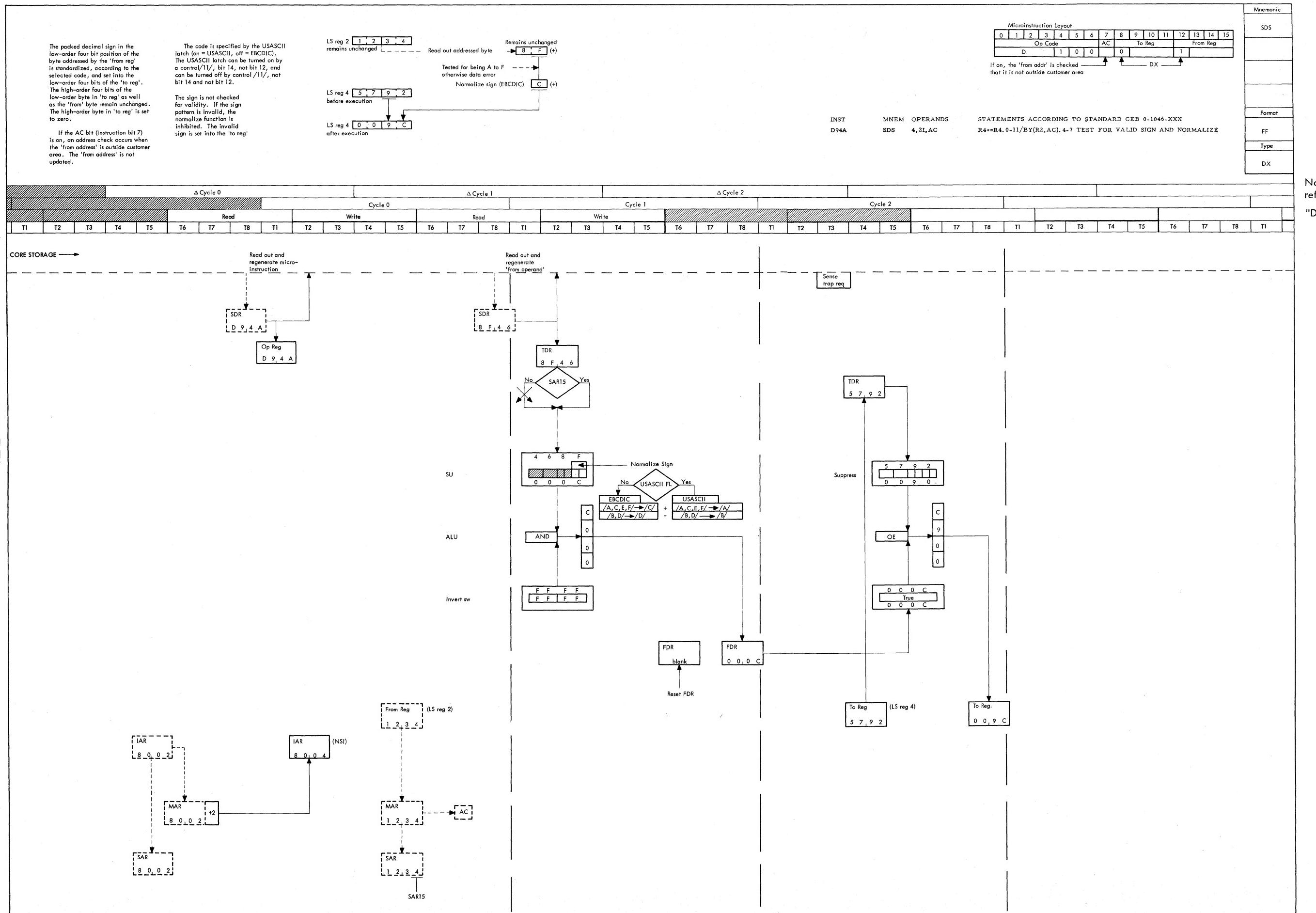


Note: For "Do not care" functions refer to timing chart below.

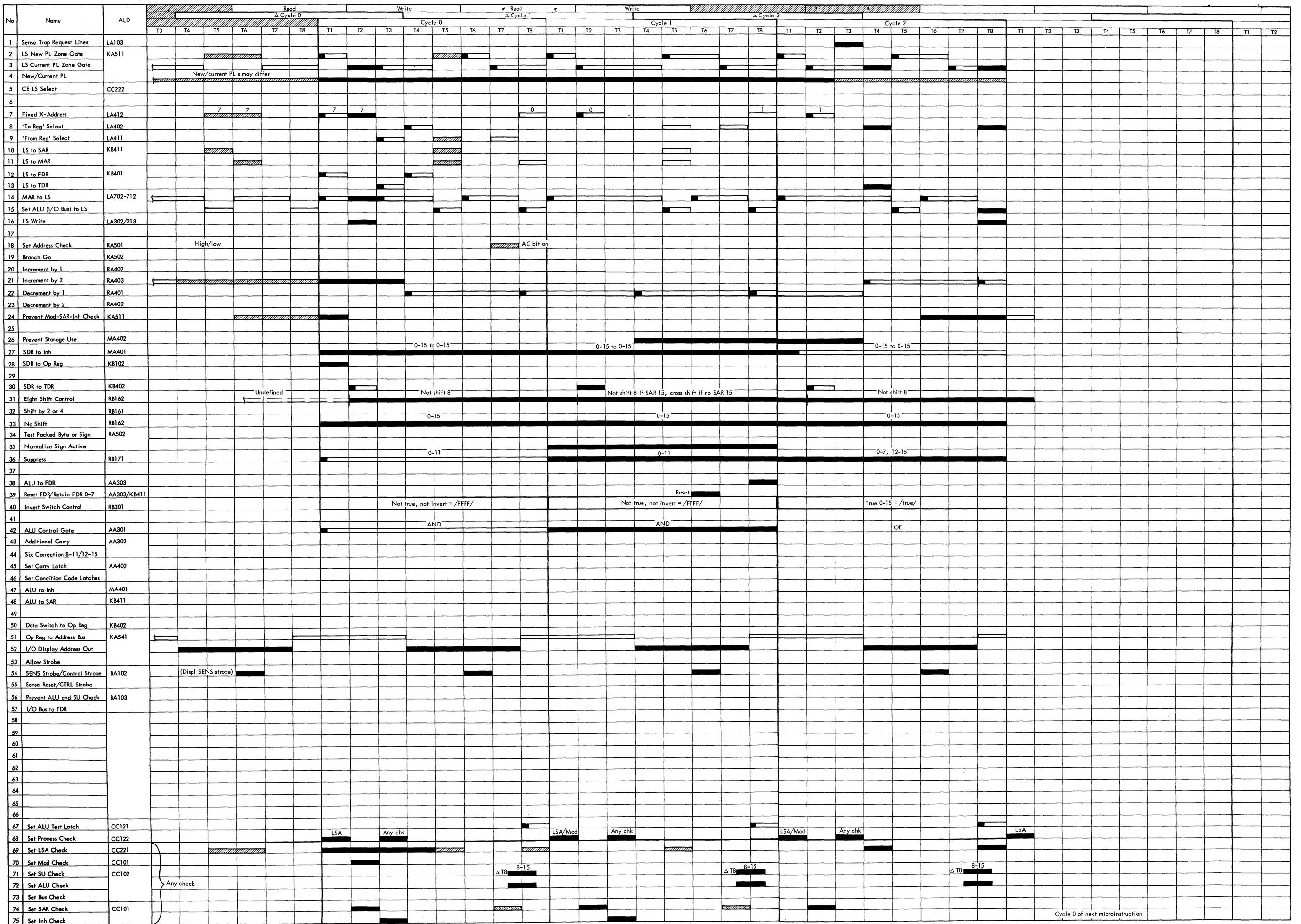
"Do not care" signals:
 ΔCycle []
 Cycle []

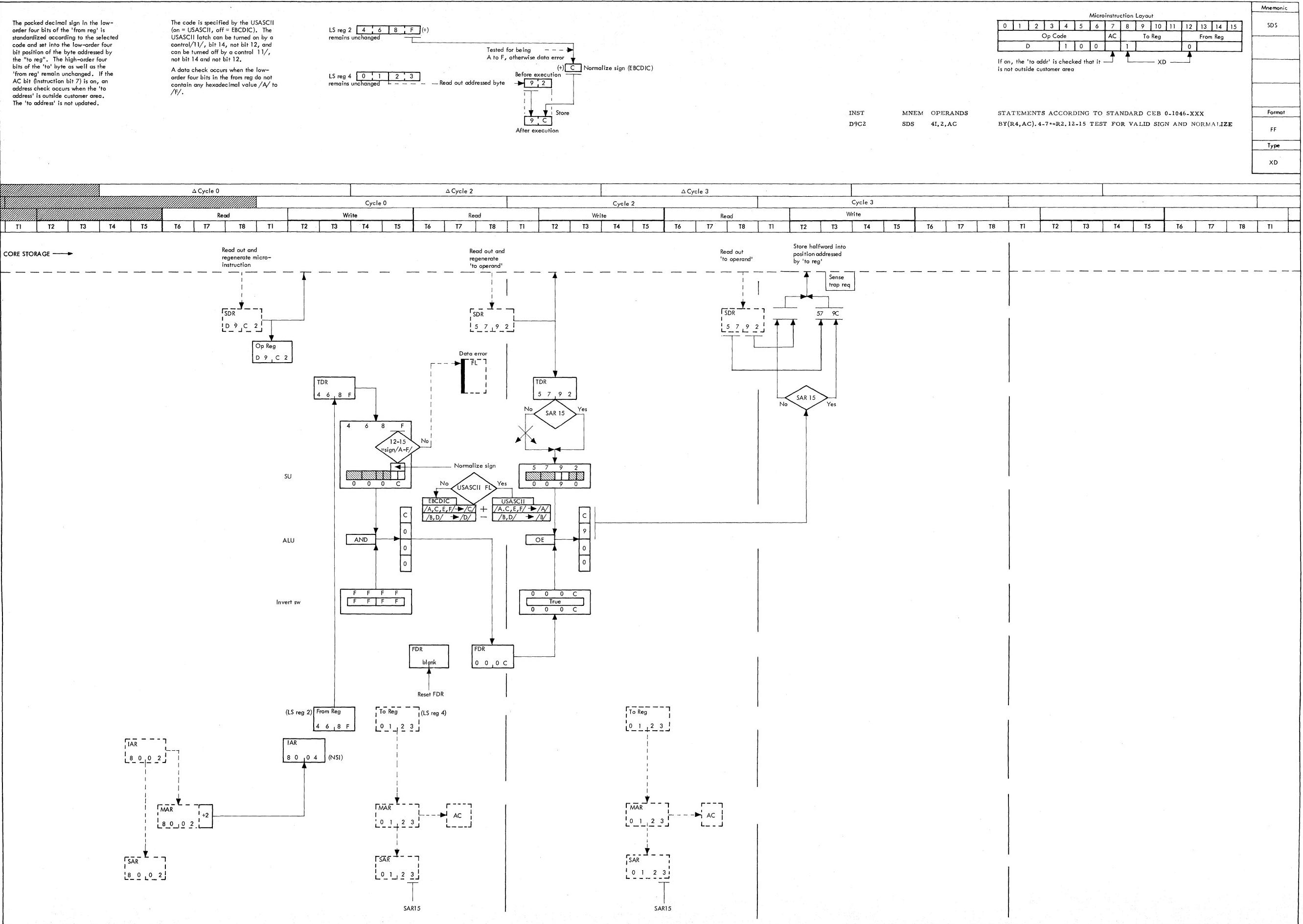
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



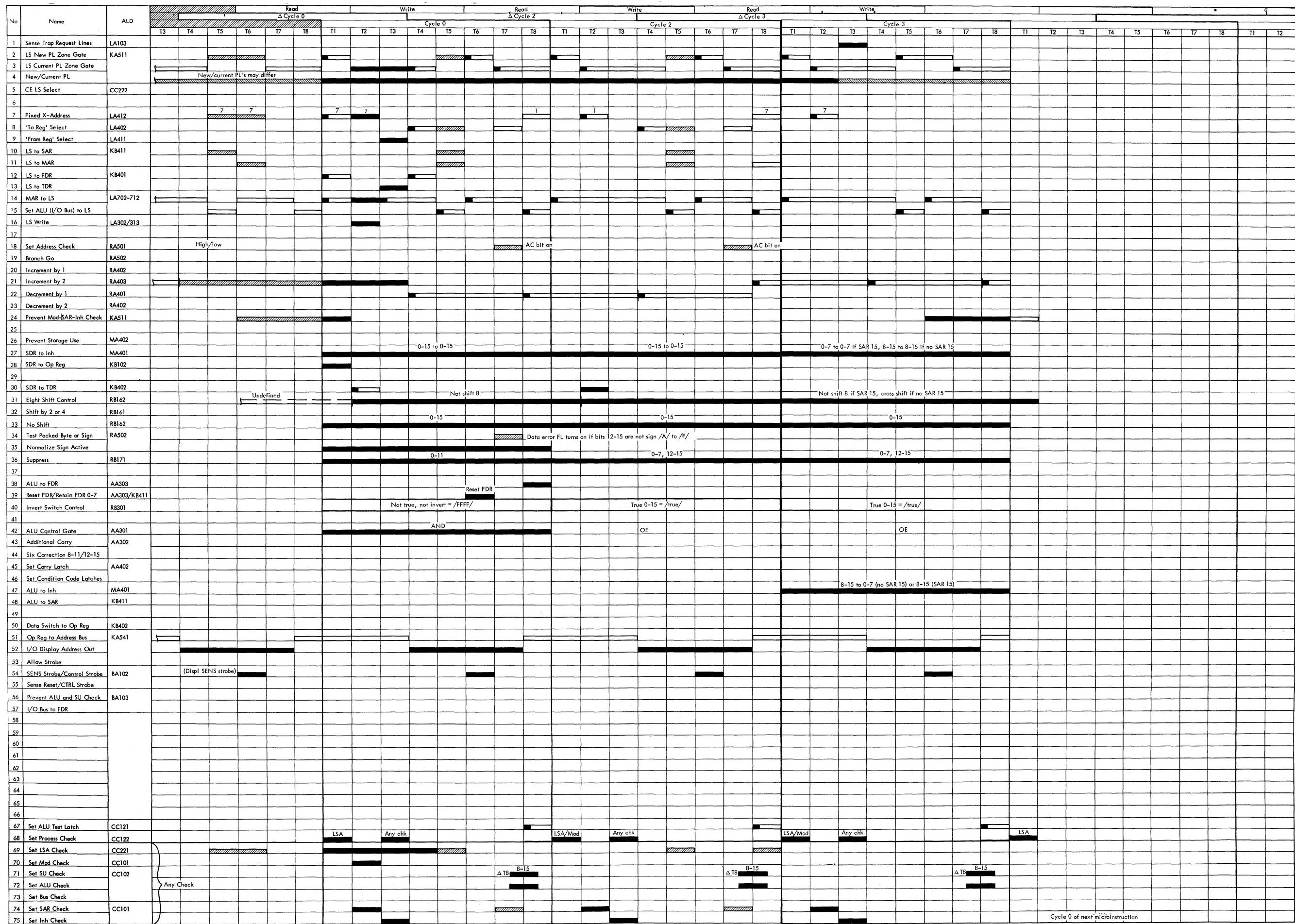


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



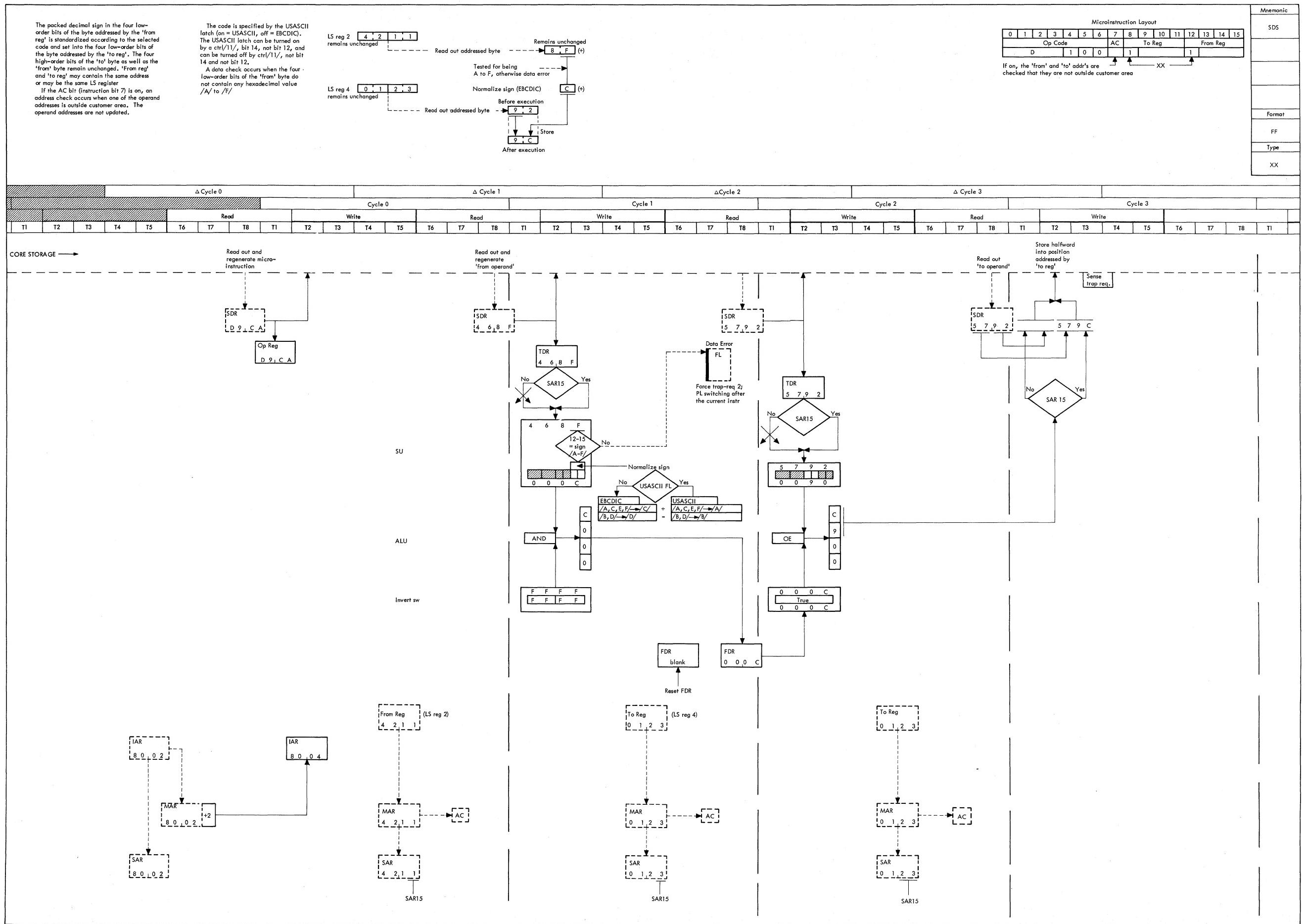


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

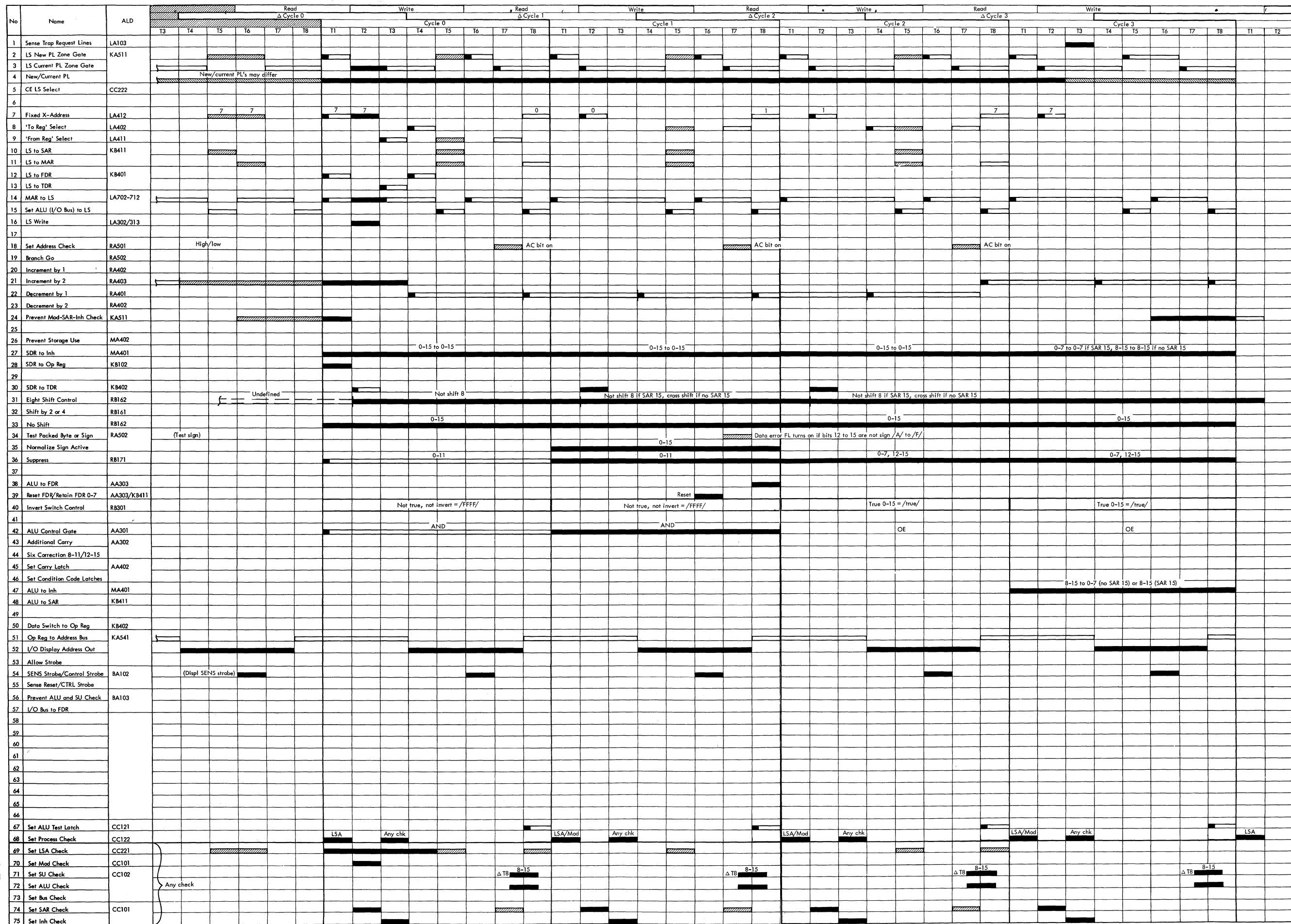


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

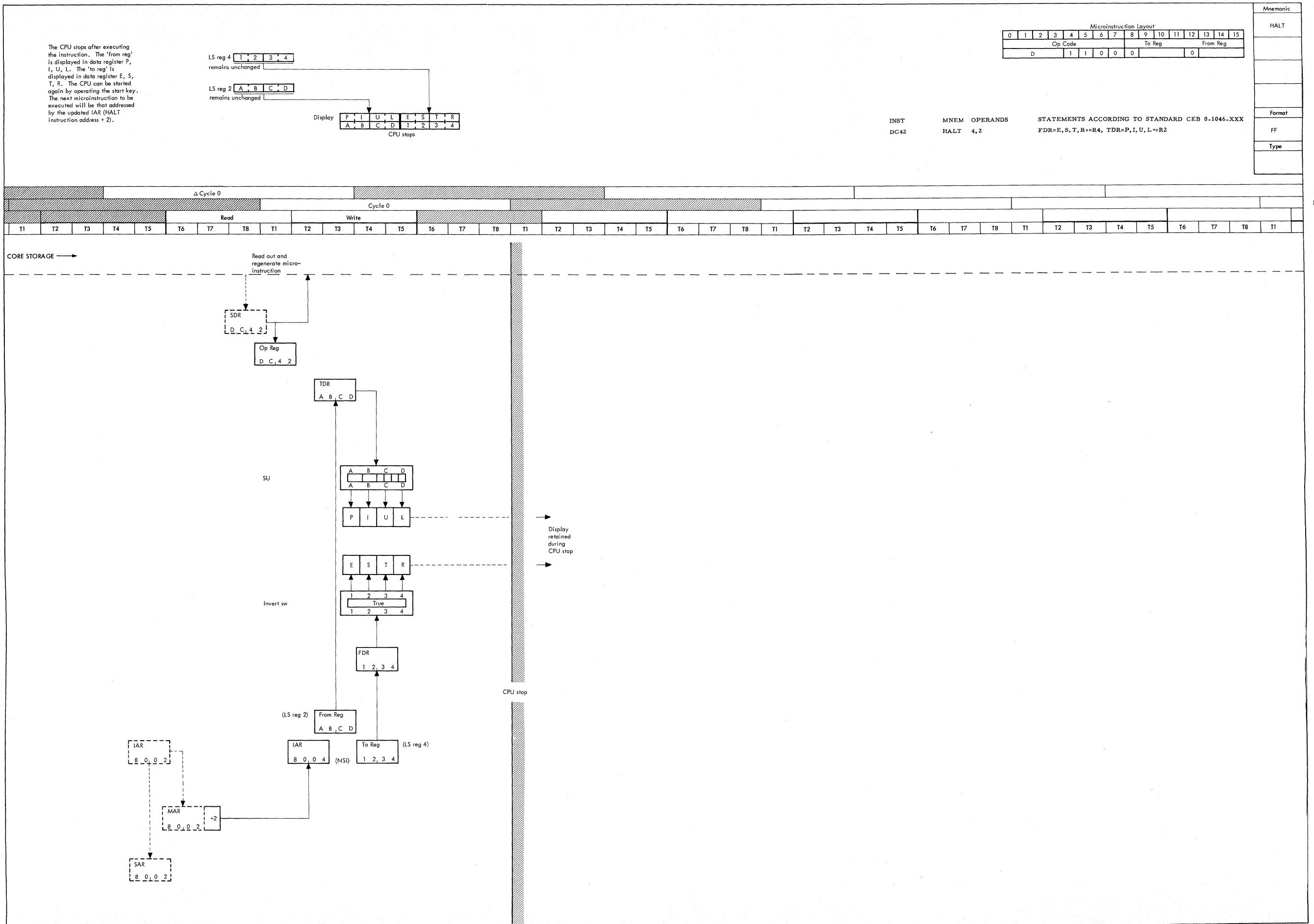


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

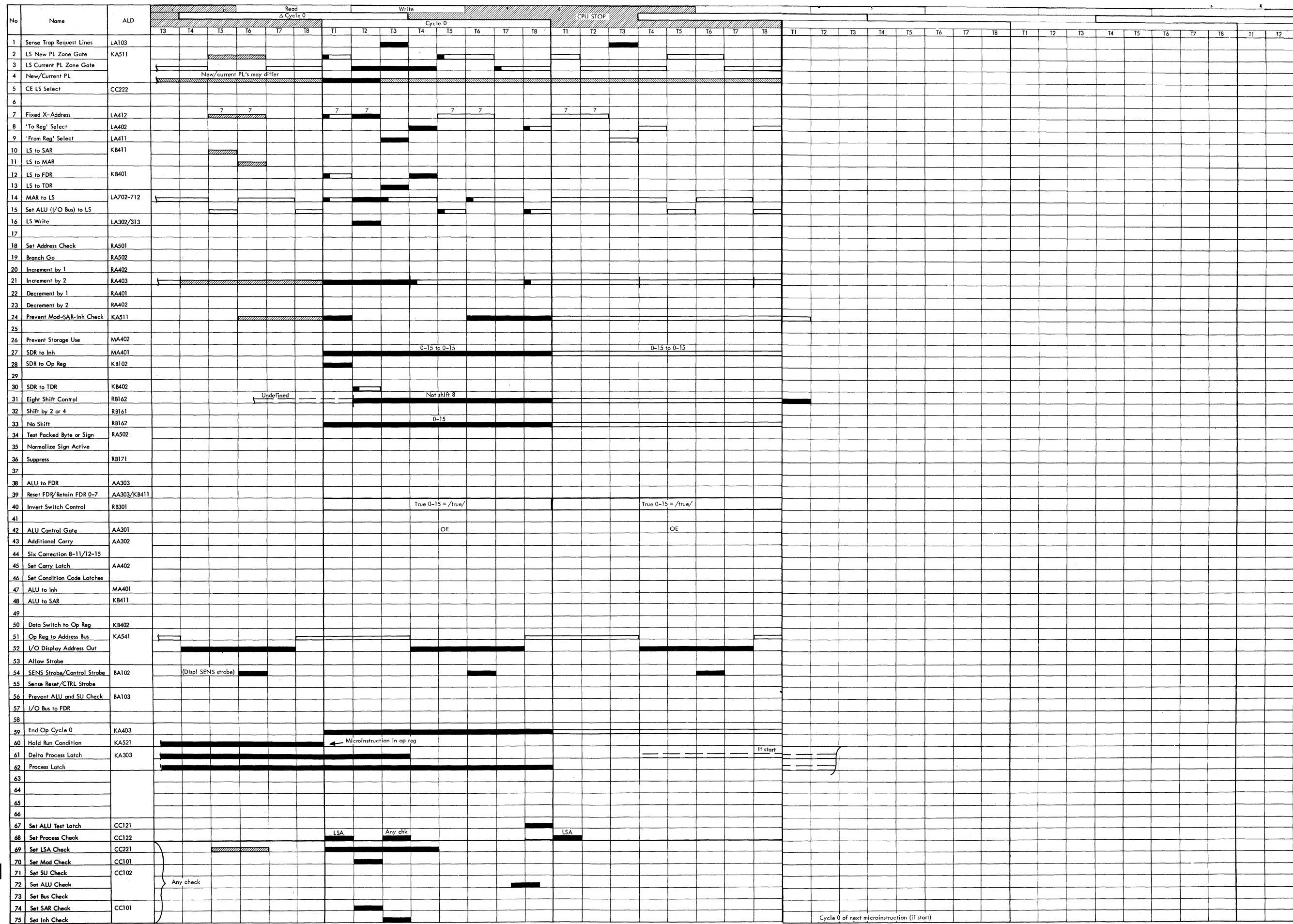


Function signals: ΔCycle Cycle

"Do not care" signals: ΔCycle Cycle

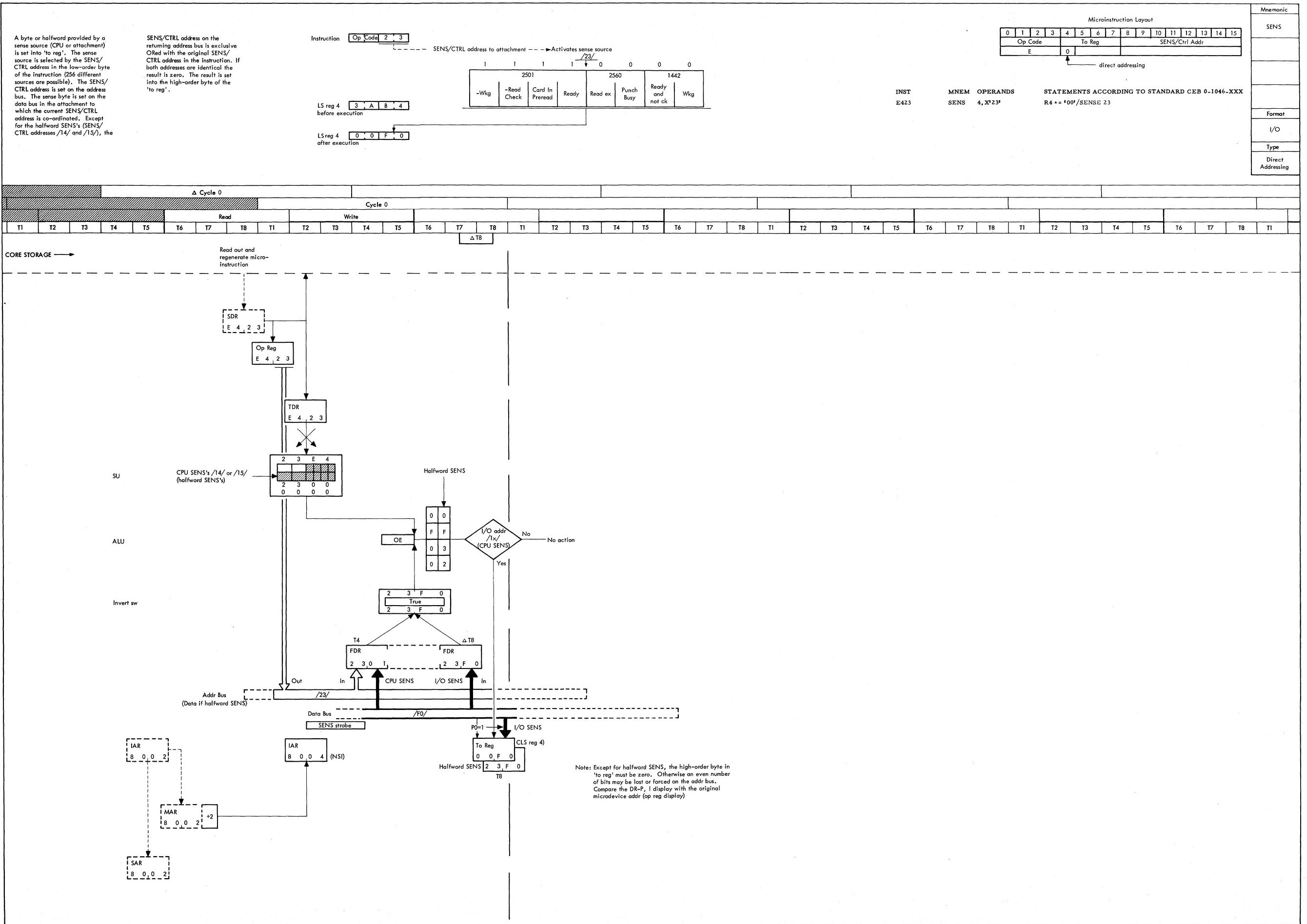


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

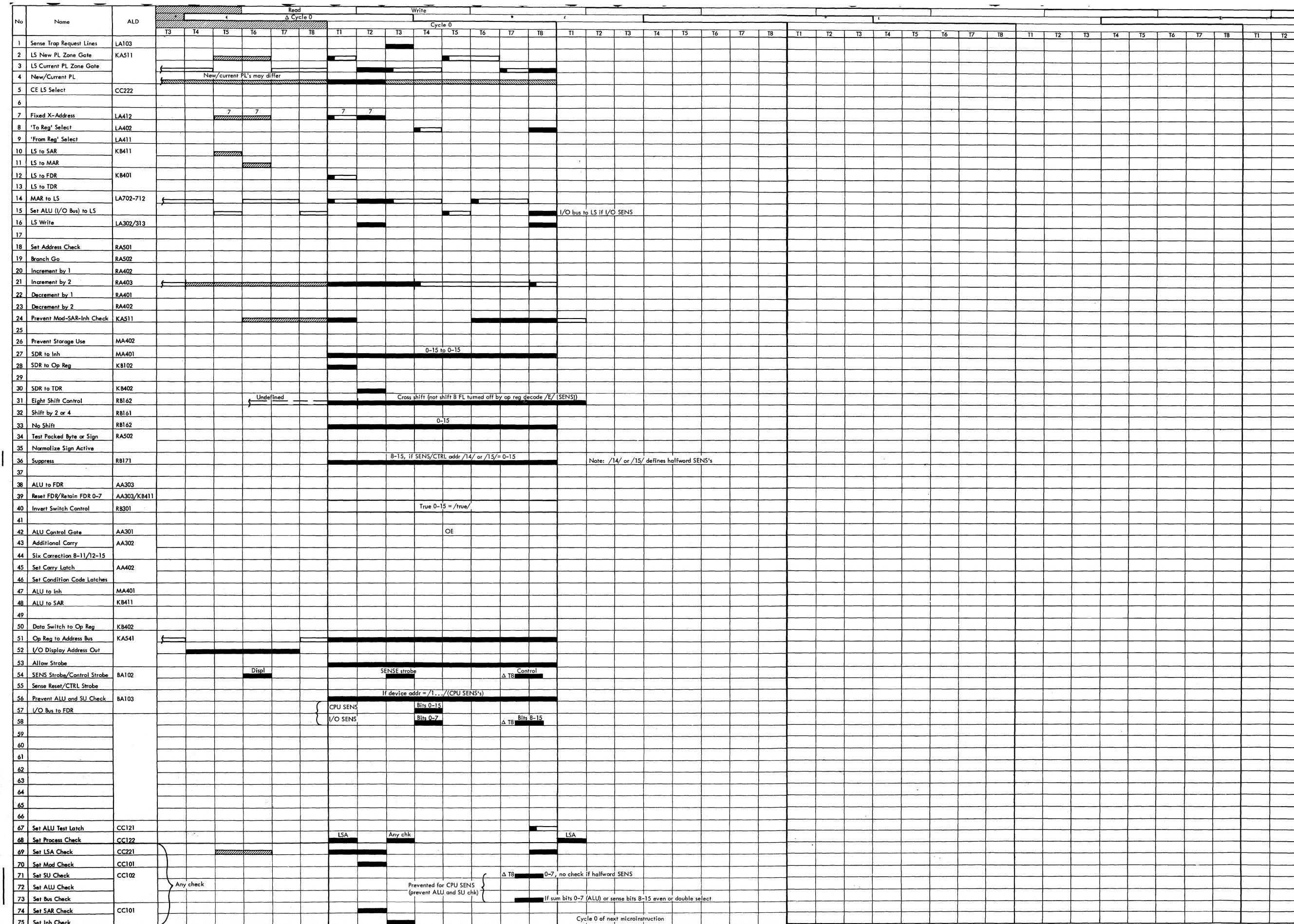


Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

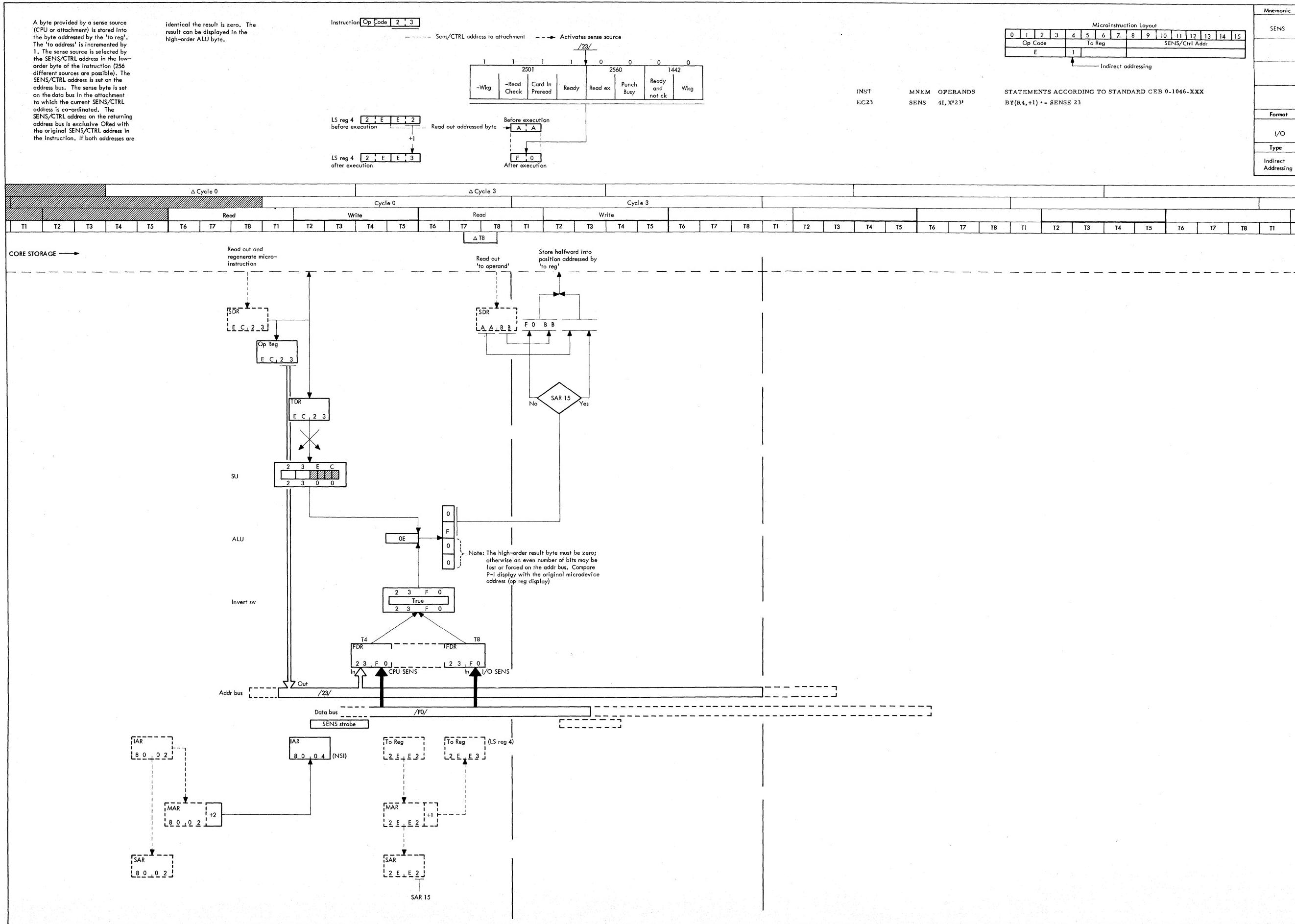


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

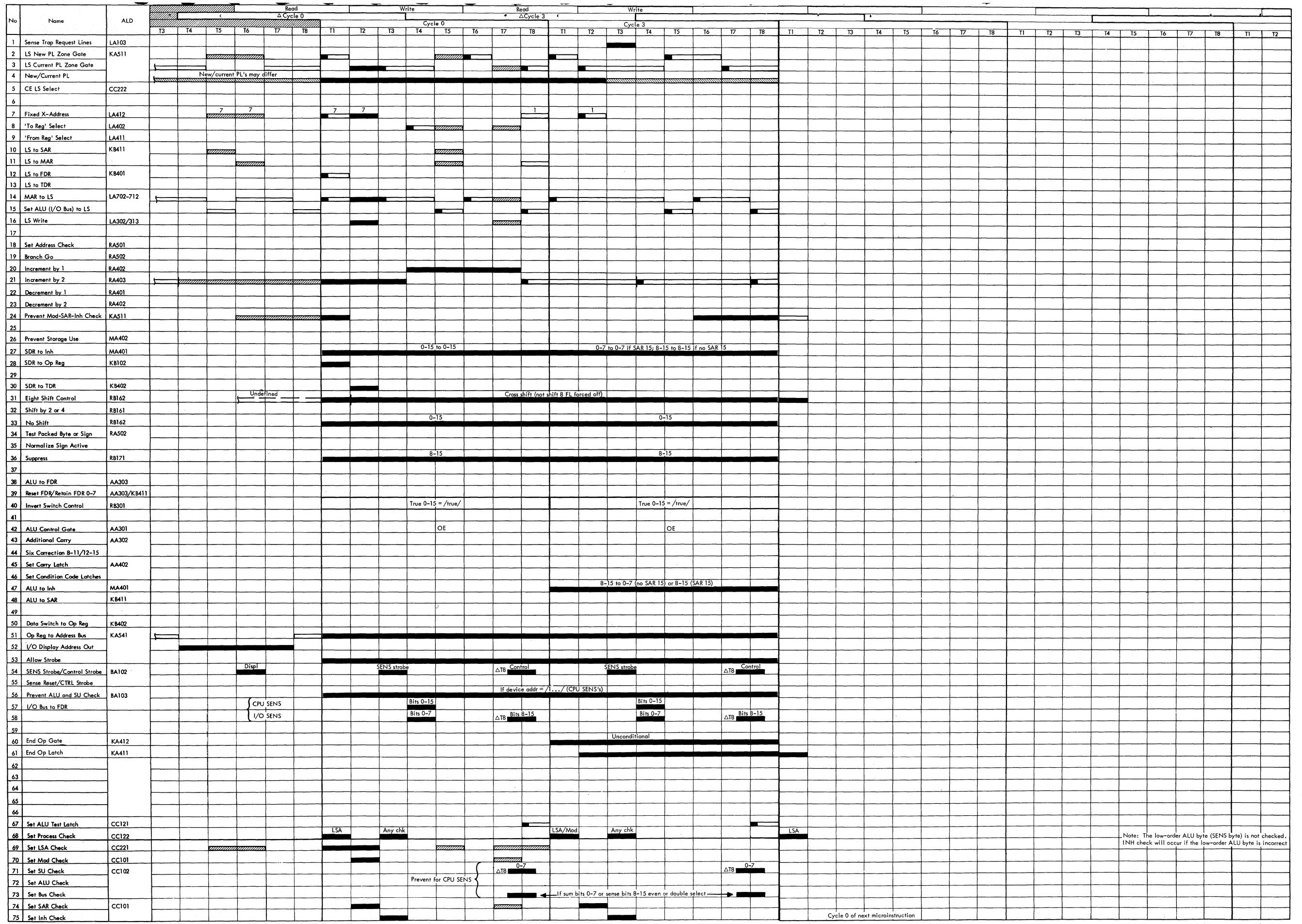
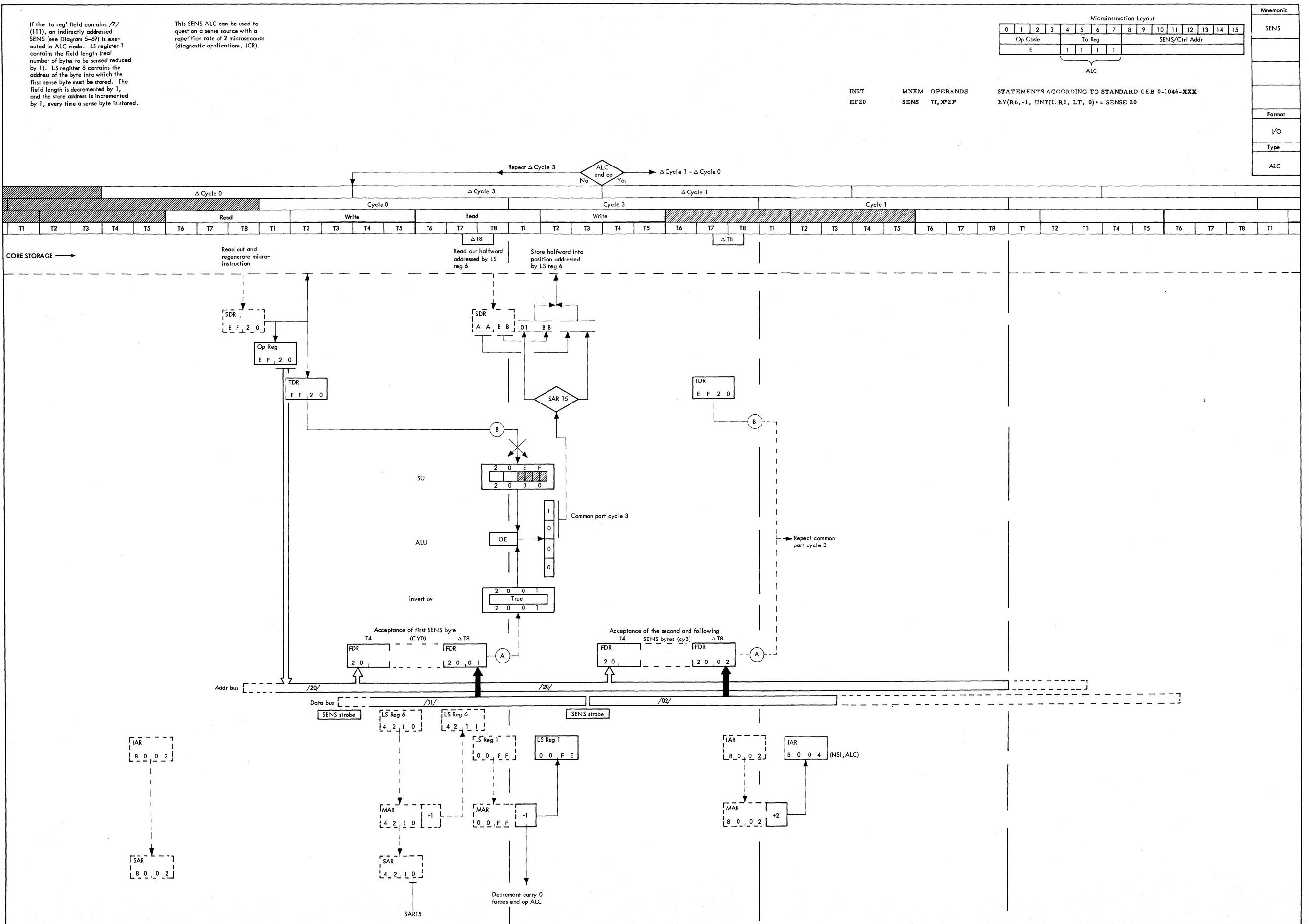


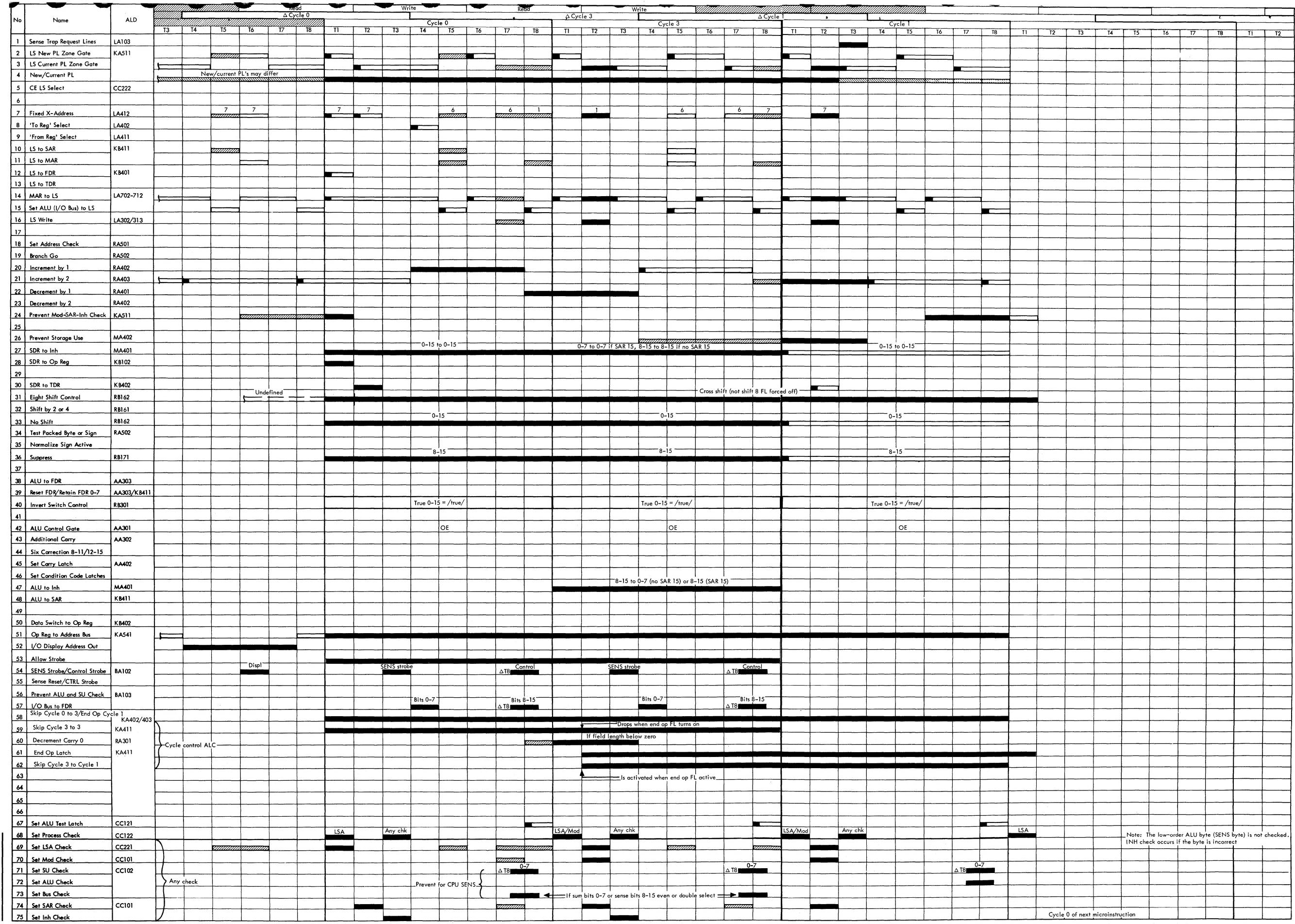
Diagram 5-68. SENS CPU I/O (Indirect Addressing) (Part 2 of 2)

(03773A)

2020 ≥ 50,000 FEMDM Vol 2 (8/69)



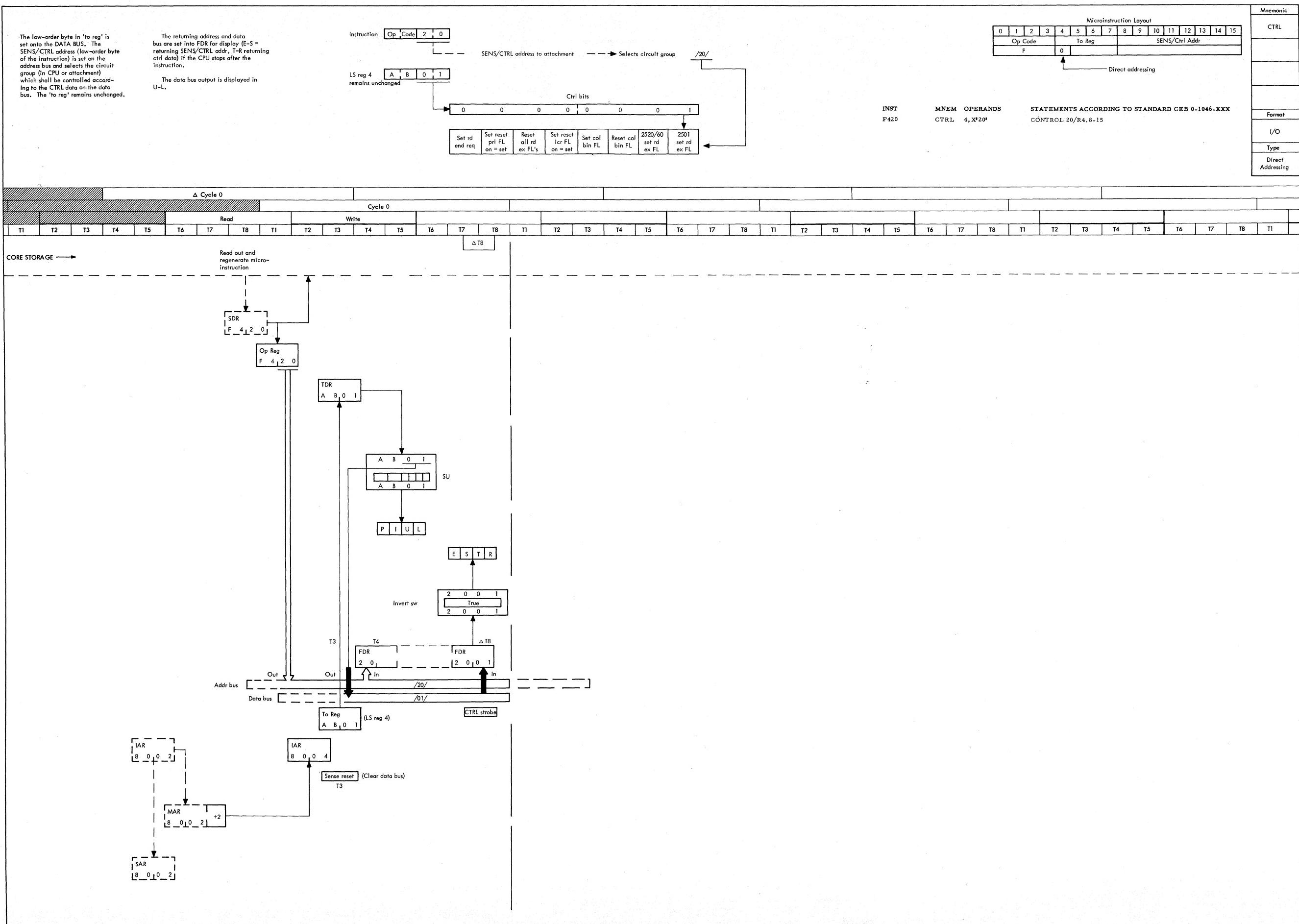
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



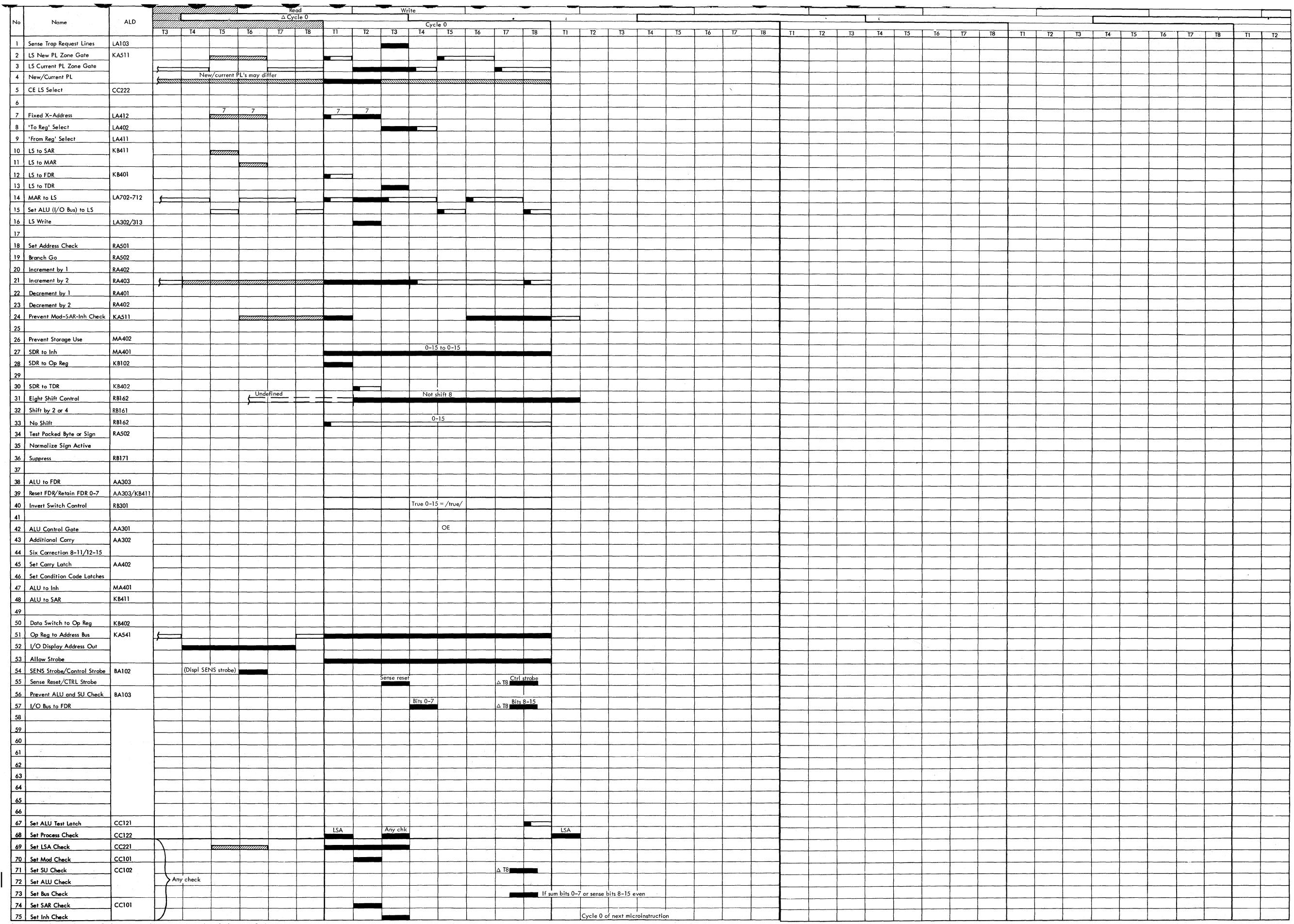
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

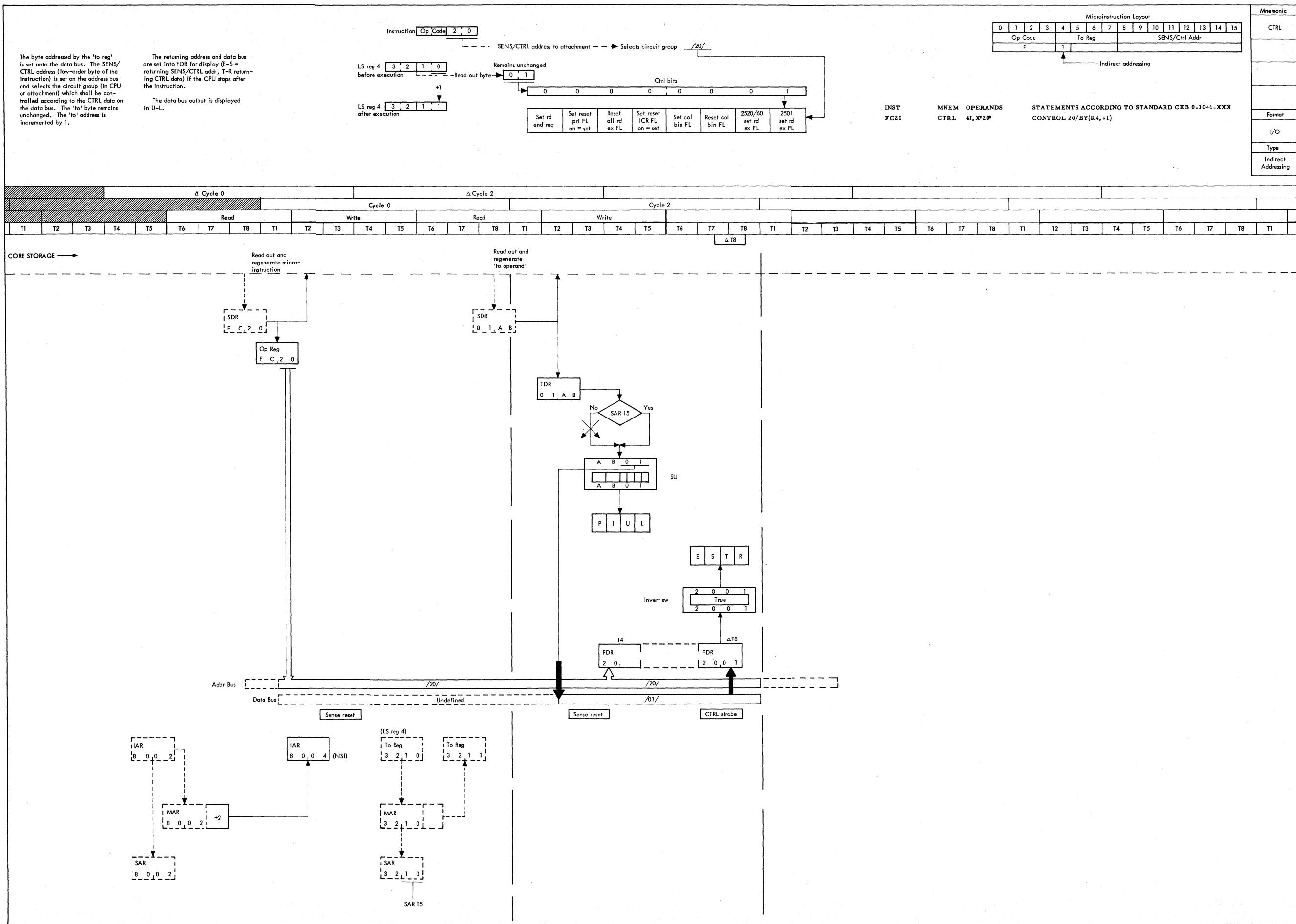
"Do not care" signals: ΔCycle Cycle

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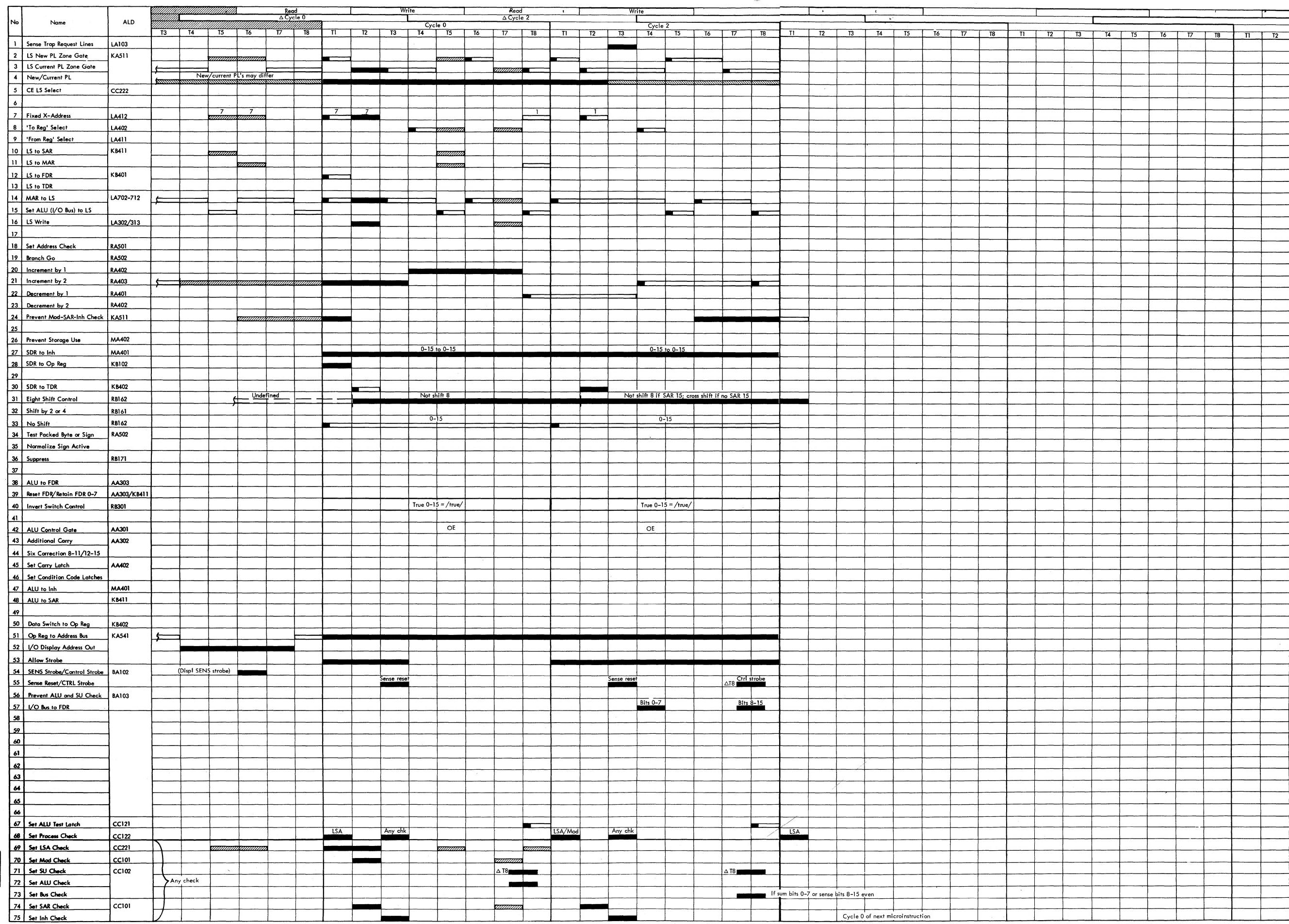


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.





Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



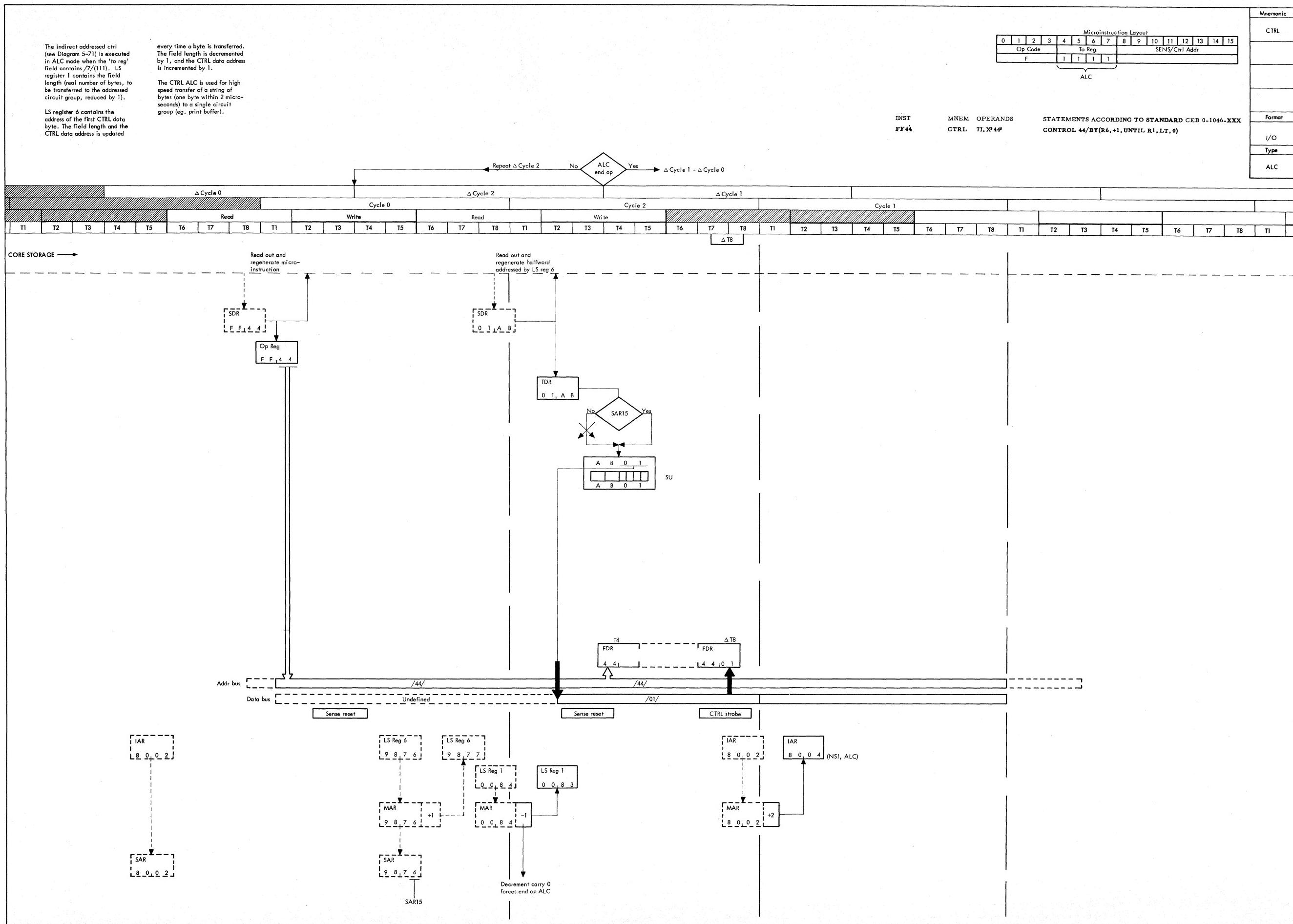
Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

● Diagram 5-71. Control I/O (Indirect Addressing) (Part 2 of 2)

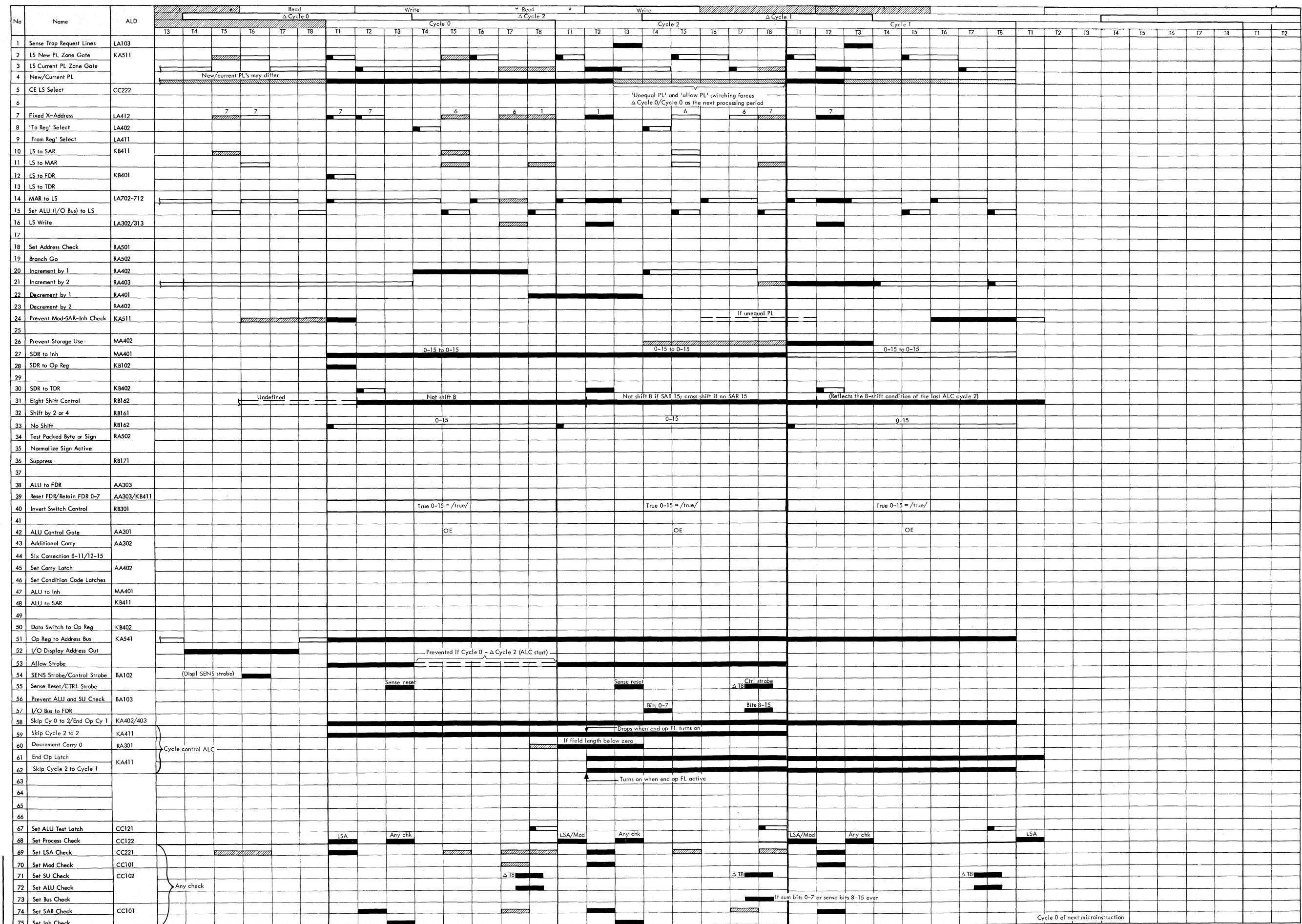
(03776A)

2020 ≥ 50,000 FEMDM Vol 2 (8/69)



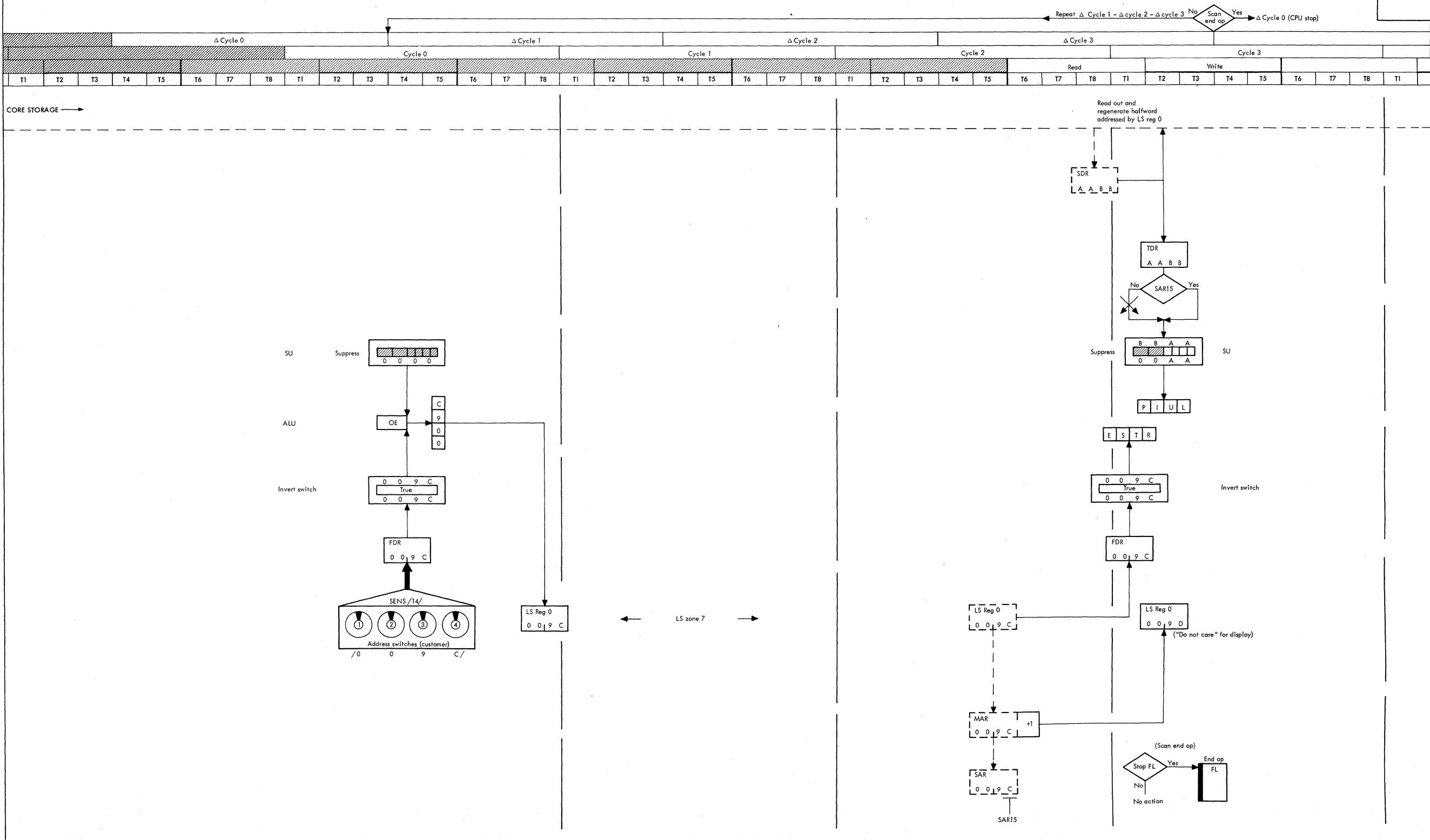
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
 Δ Cycle Cycle

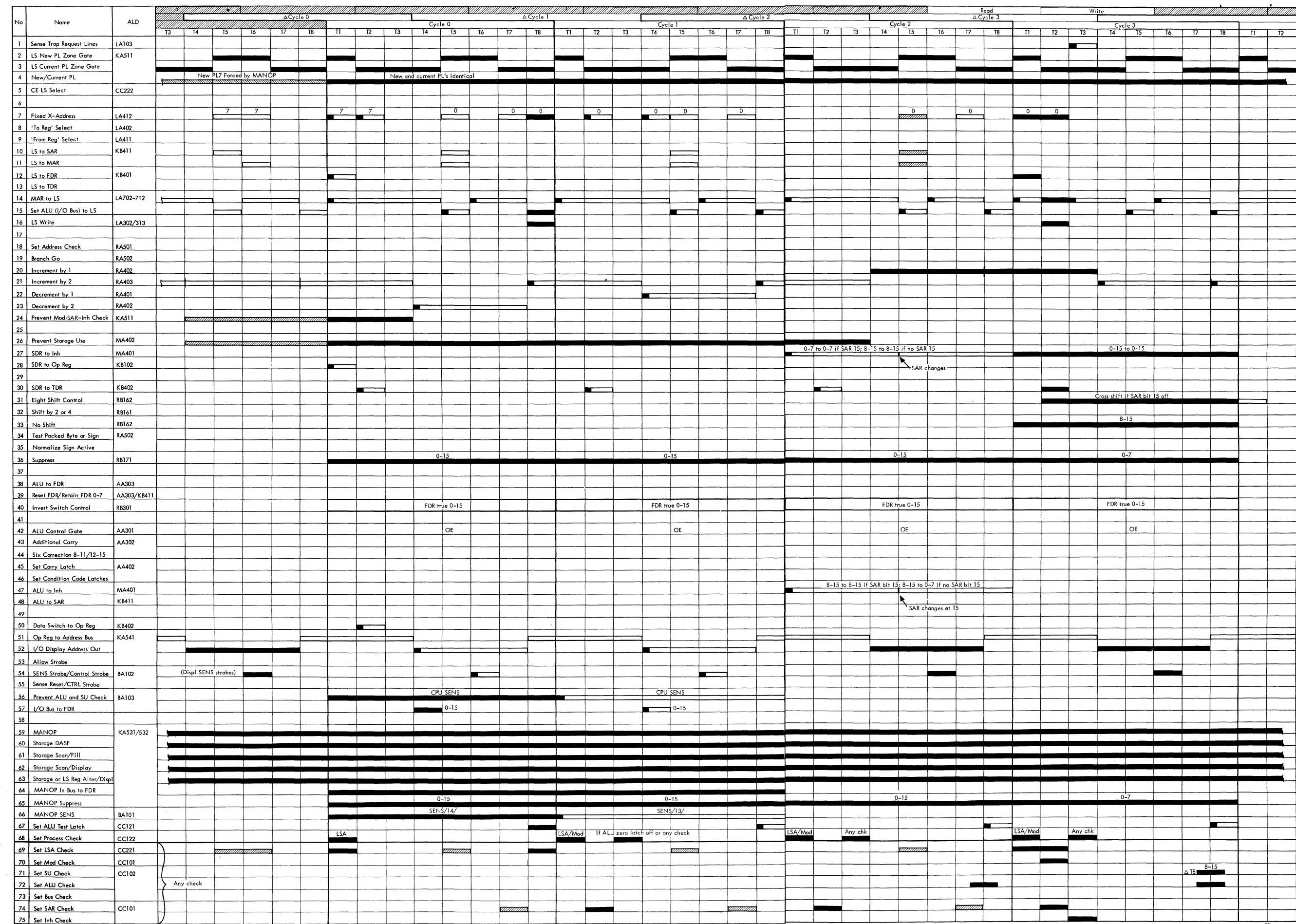


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Mnemonic
Format
Type



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

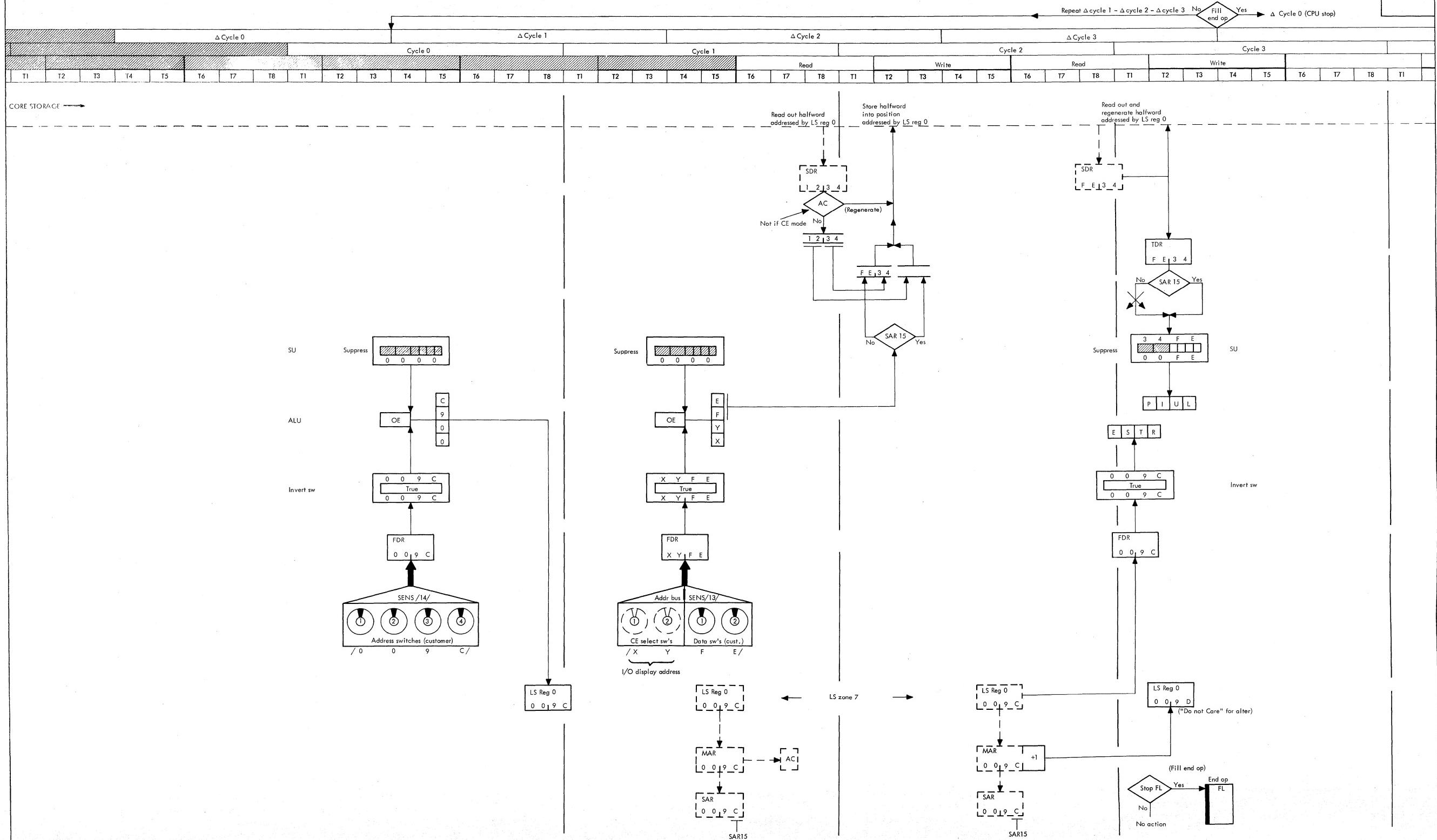
"Do not care" signals: ΔCycle Cycle

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Mnemonic
Format
Type

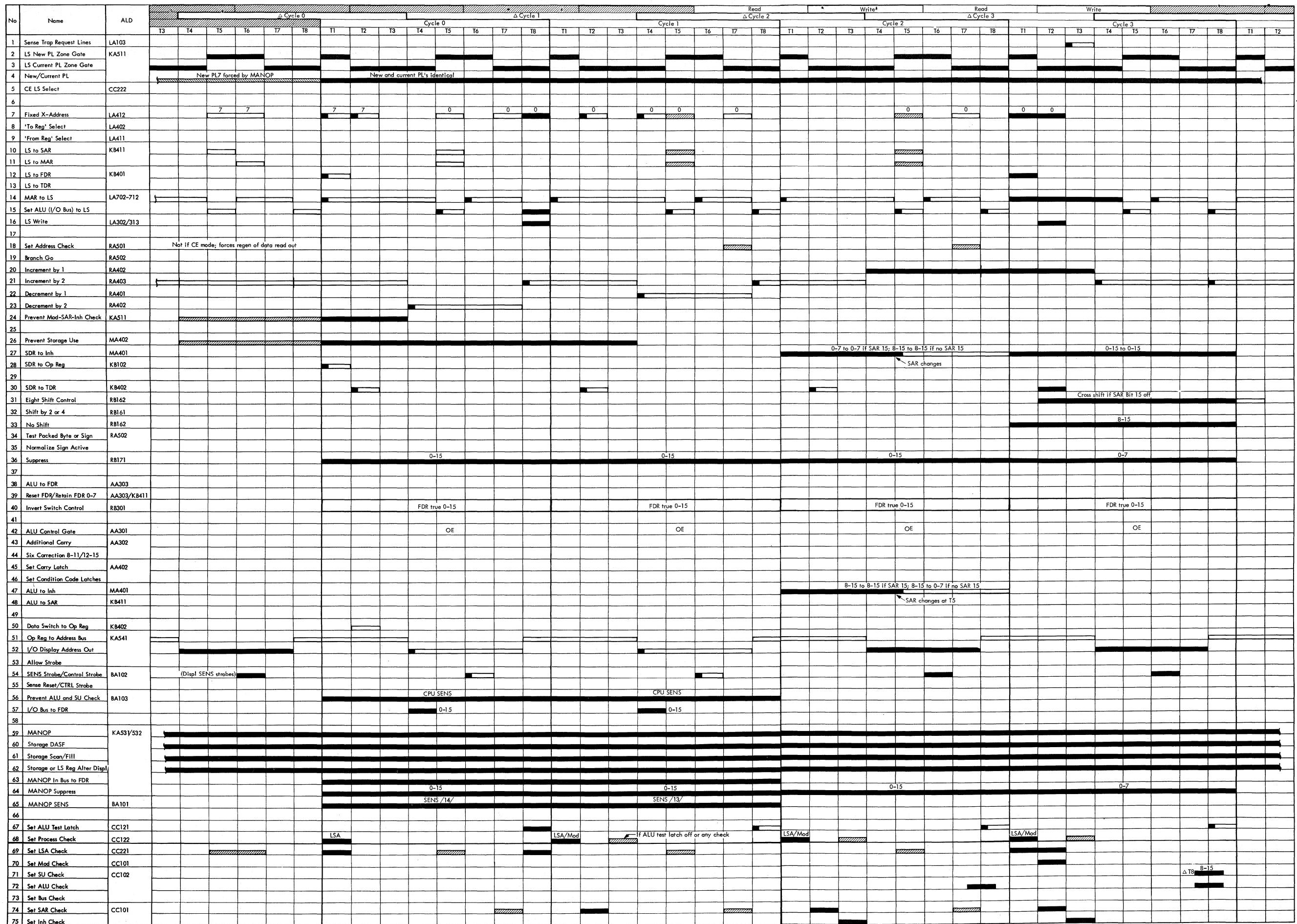
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
 ΔCycle []
 Cycle []



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-74. Storage Alter/Fill (Part 1 of 2) (03779) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)



Function signals: ΔCycle █ Cycle █ "Do not care" signals: ΔCycle █ Cycle █

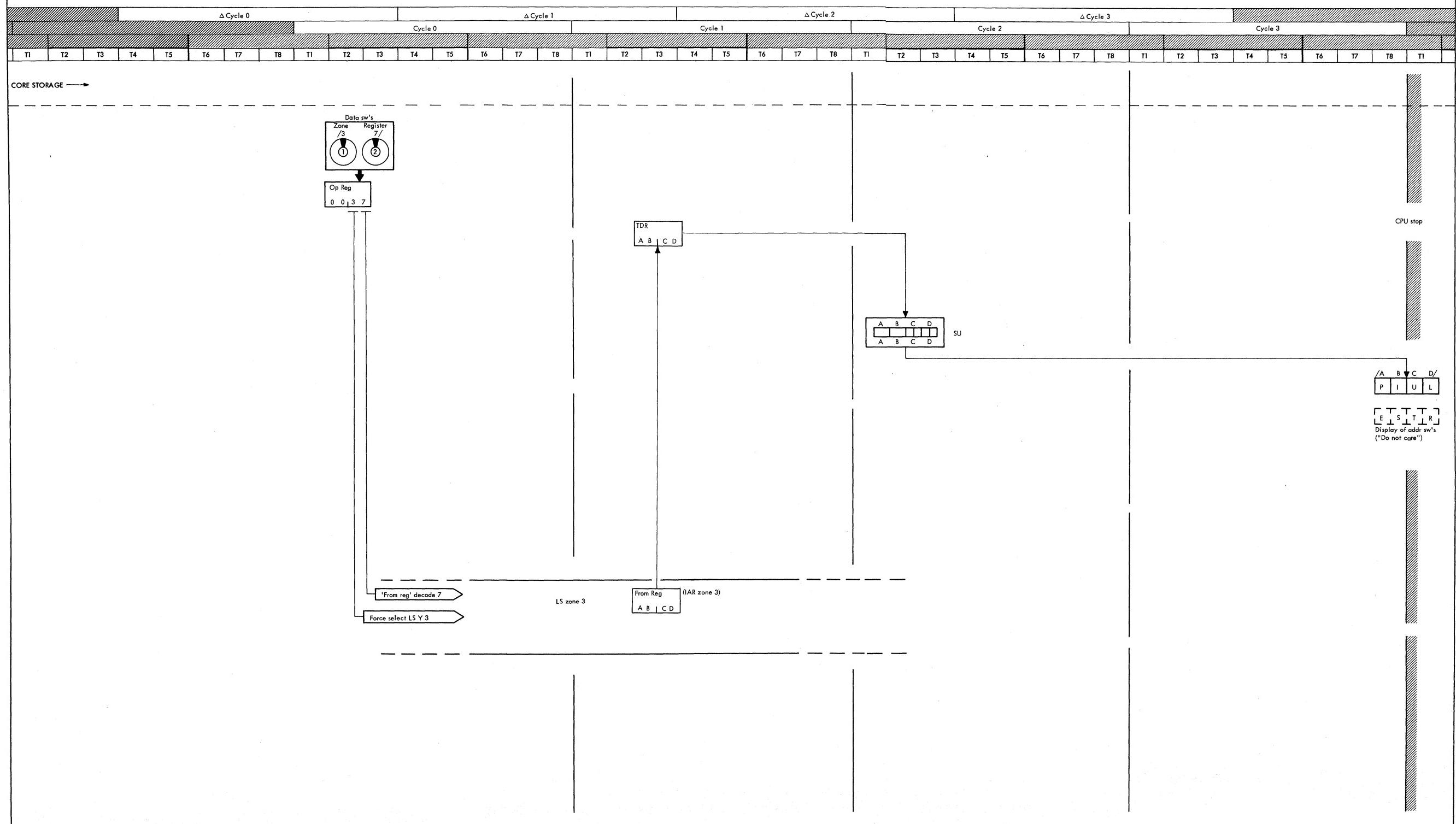
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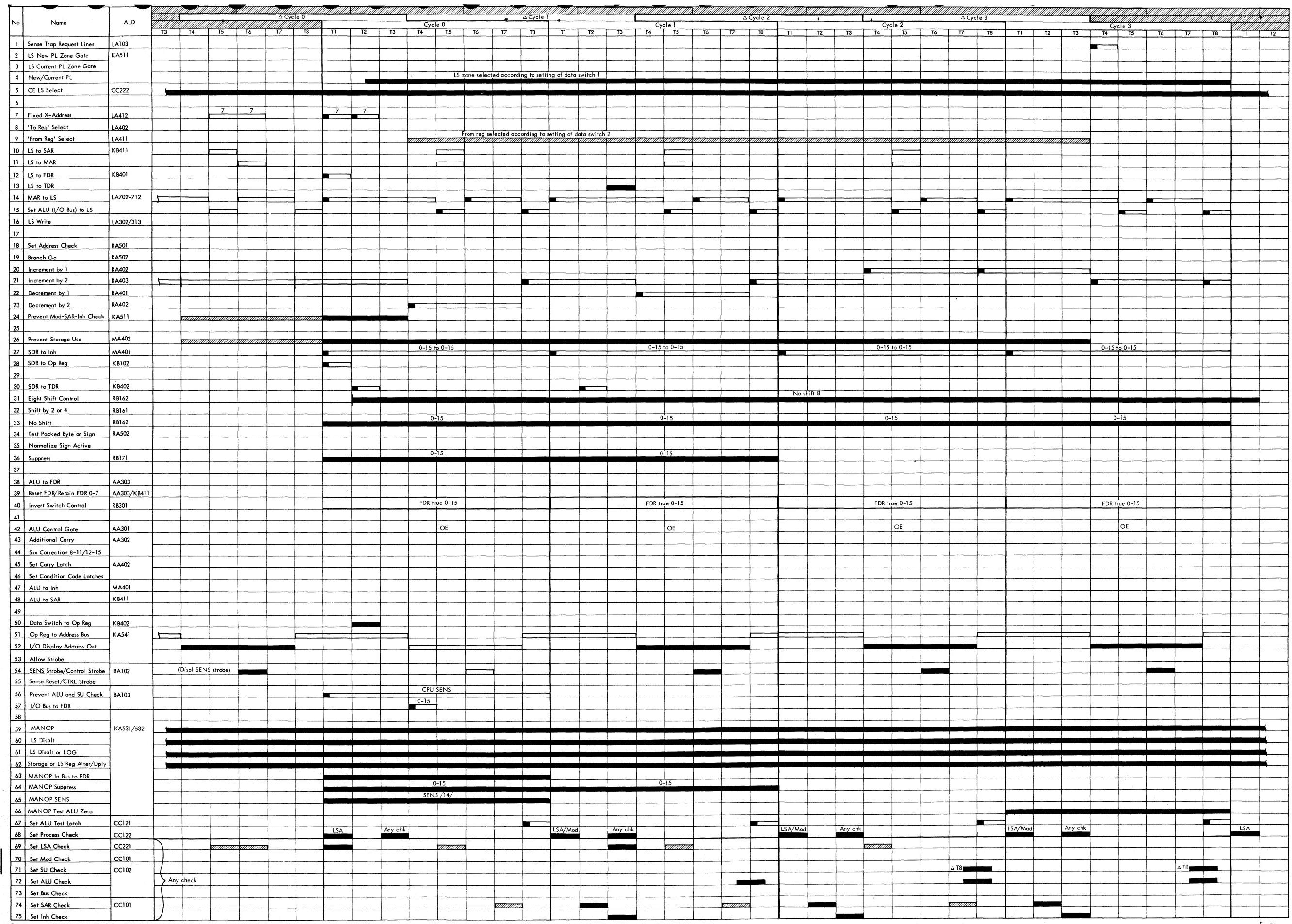
Mnemonic
Format
Type

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:

ΔCycle Cycle





Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

"Do not care" signals: Δ Cycle Cycle

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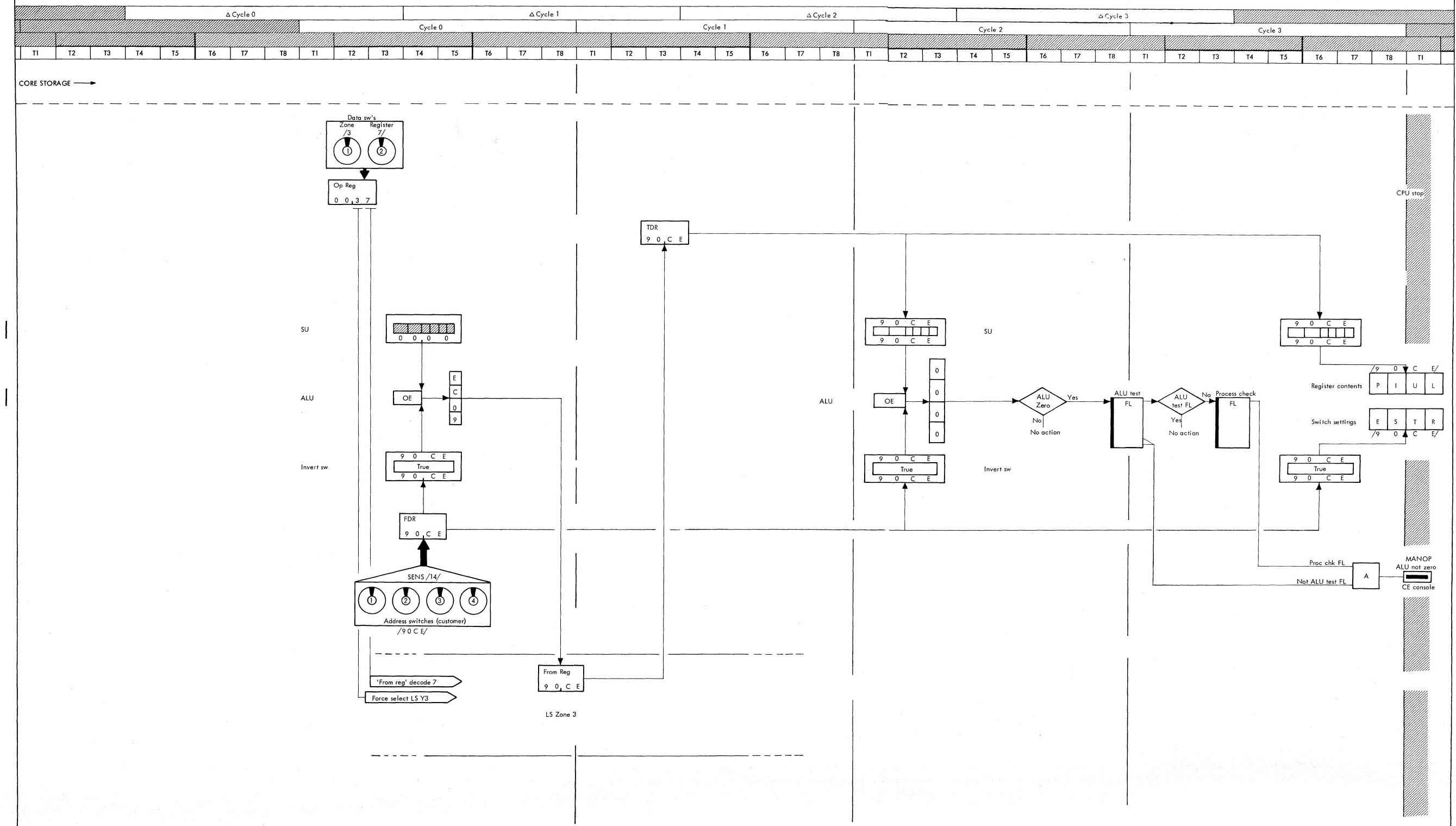
Mnemonic
Format
Type

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:

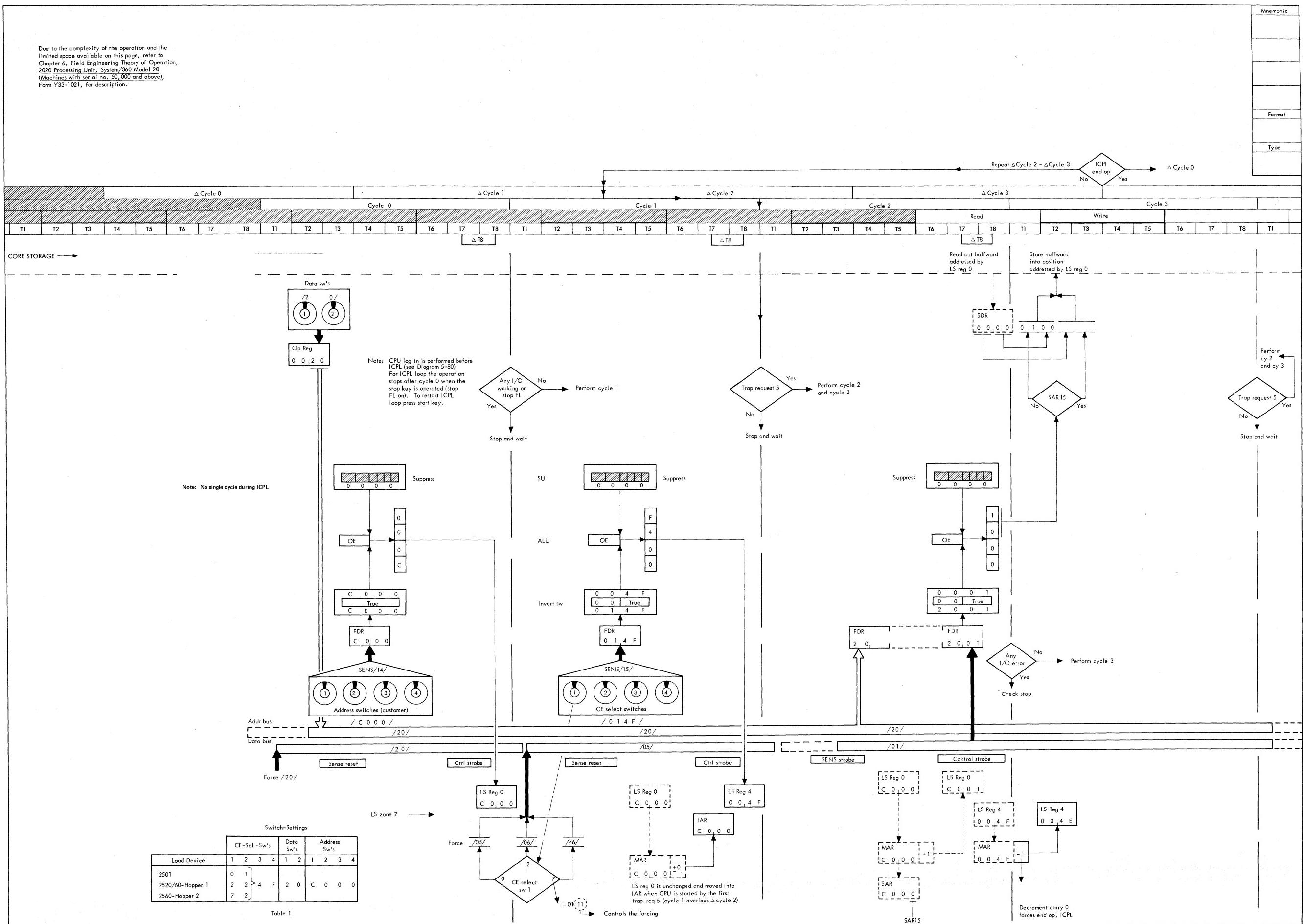
ΔCycle

Cycle

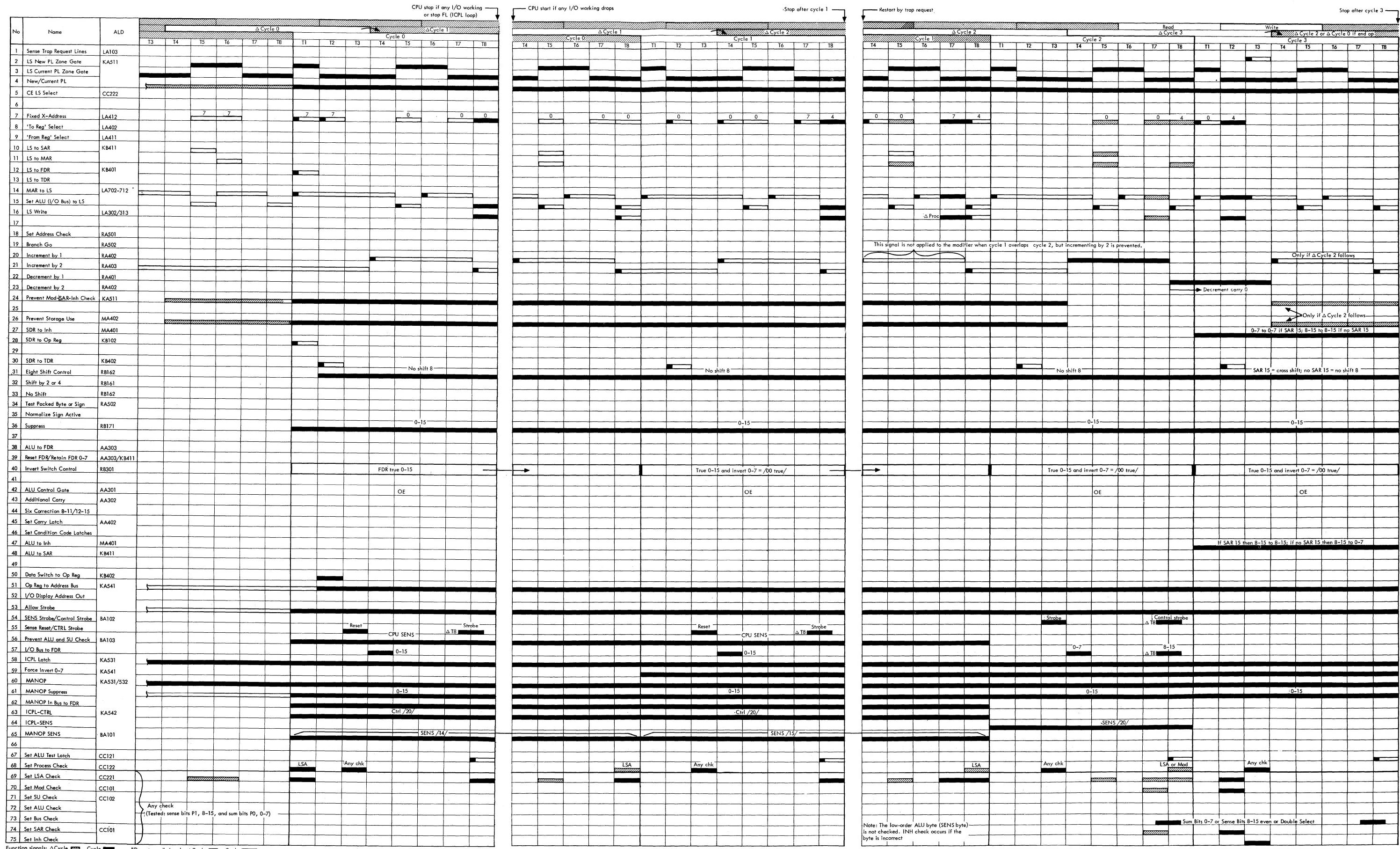


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD	Δ Cycle 0						Δ Cycle 1						Δ Cycle 2						Δ Cycle 3												
			T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1	T2	T3	T4	T5	T6	T7	T8	T1
1	Sense Trap Request Lines	LA103																															
2	LS New PL Zone Gate	KA511																															
3	LS Current PL Zone Gate																																
4	New/Current PL																																
5	CE LS Select	CC222																															
6																																	
7	Fixed X-Address	LA412		7	7					7	7																						
8	'To Reg' Select	LA402																															
9	'From Reg' Select	LA411																															
10	LS to SAR	KB411																															
11	LS to MAR																																
12	LS to FDR	KB401																															
13	LS to TDR																																
14	MAR to LS	LA702-712																															
15	Set ALU (I/O Bus) to LS																																
16	LS Write	LA302/313																															
17																																	
18	Set Address Check	RA501																															
19	Branch Go	RA502																															
20	Increment by 1	RA402																															
21	Increment by 2	RA403																															
22	Decrement by 1	RA401																															
23	Decrement by 2	RA402																															
24	Prevent Mod-SAR-Inh Check	KA511																															
25																																	
26	Prevent Storage Use	MA402																															
27	SDR to Inh	MA401																															
28	SDR to Op Reg	KB102																															
29																																	
30	SDR to TDR	KB402																															
31	Eight Shift Control	RB162																															
32	Shift by 2 or 4	RB161																															
33	No Shift	RB162																															
34	Test Packed Byte or Sign	RA502																															
35	Normalize Sign Active																																
36	Suppress	RB171																															
37																																	
38	ALU to FDR	AA303																															
39	Reset FDR/Retain FDR 0-7	AA303/KB411																															
40	Invert Switch Control	RB301																															
41																																	
42	ALU Control Gate	AA301																															
43	Additional Carry	AA302																															
44	Six Correction 8-11/12-15																																
45	Set Carry Latch	AA402																															

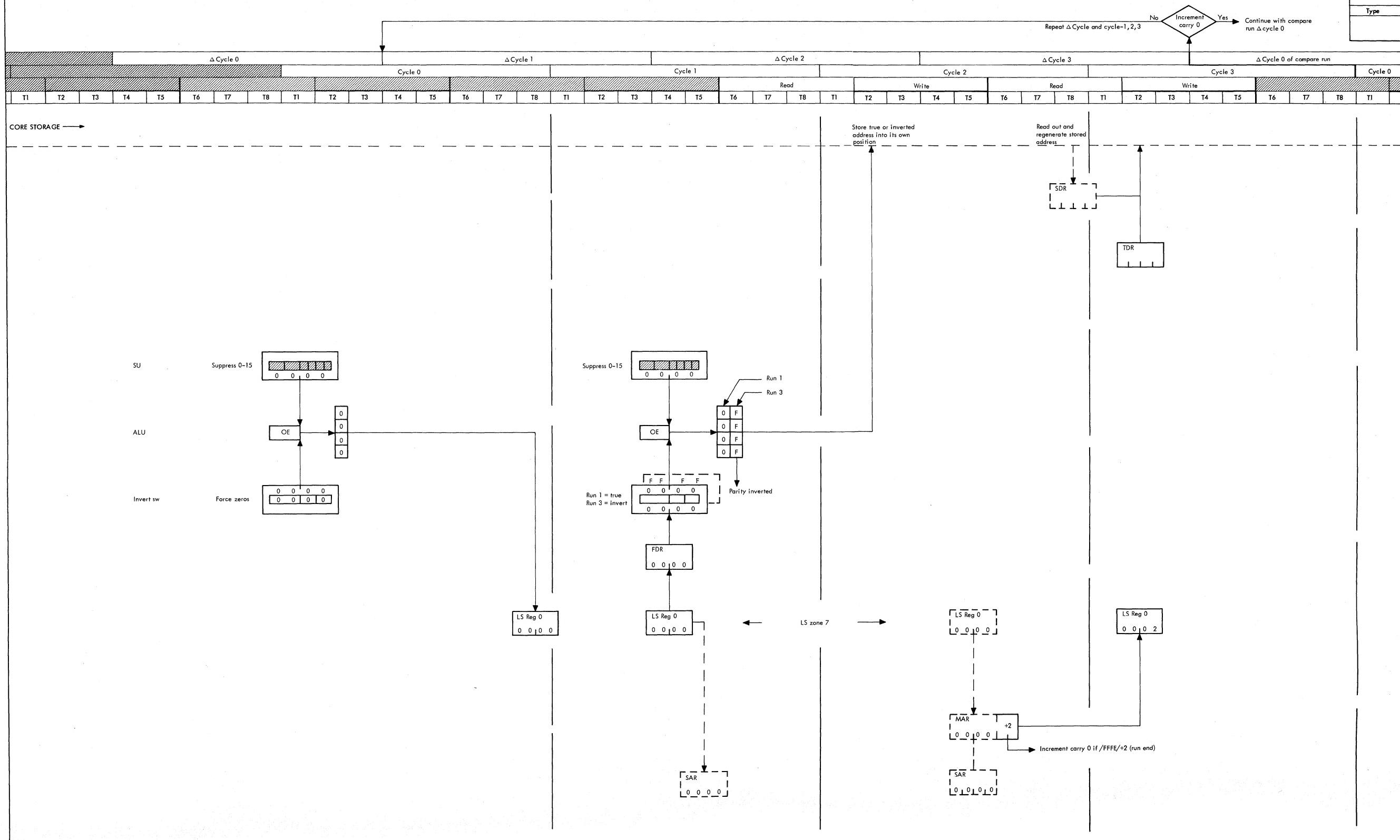


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

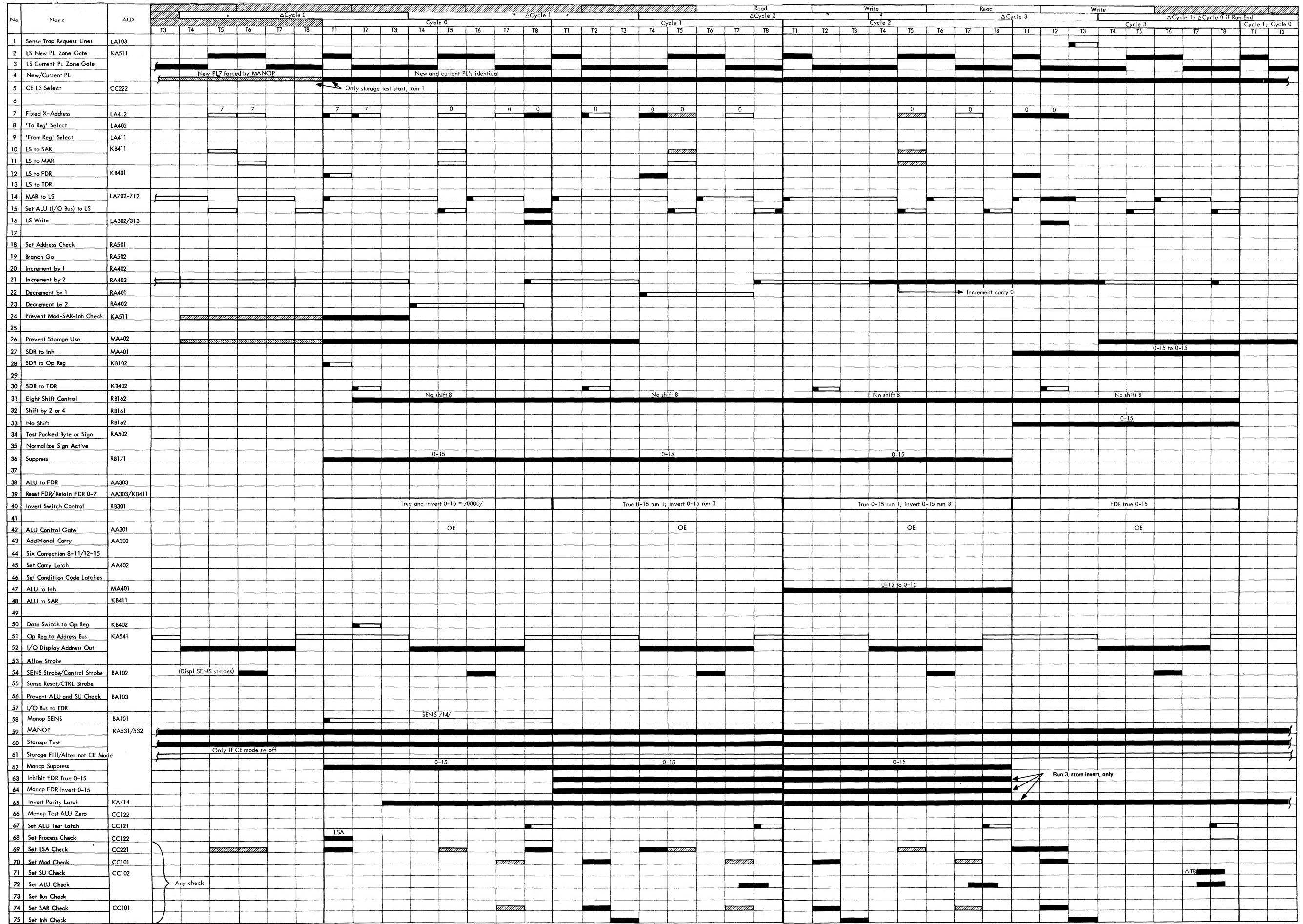


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Mnemonic
Format
Type



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle Cycle "Do not care" signals: Δ Cycle Cycle

— 1 —

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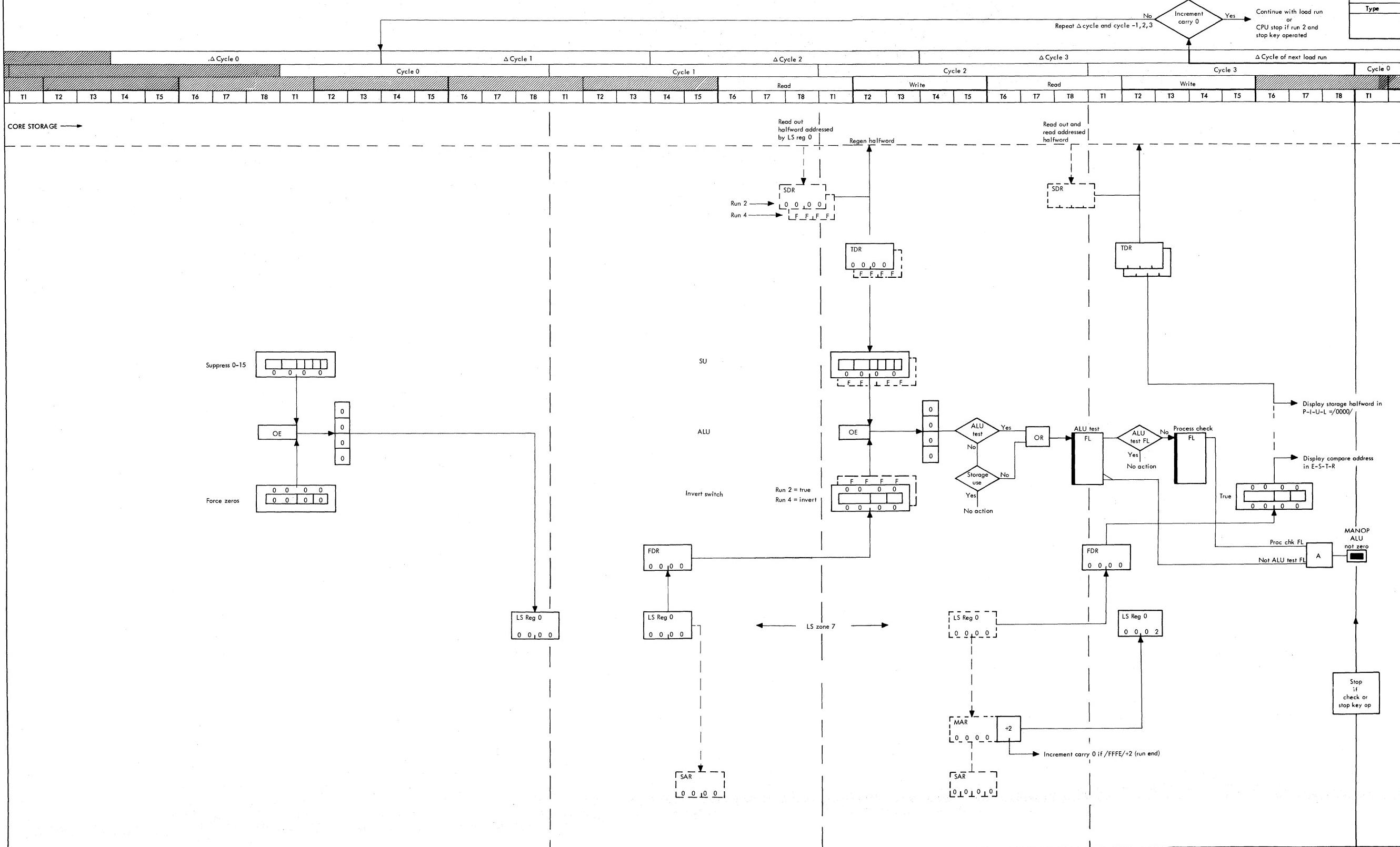
Mnemonic
Format
Type

Repeat Δ cycle and cycle -1, 2, 3
No
Increment carry 0
Yes
Continue with load run or CPU stop if run 2 and stop key operated

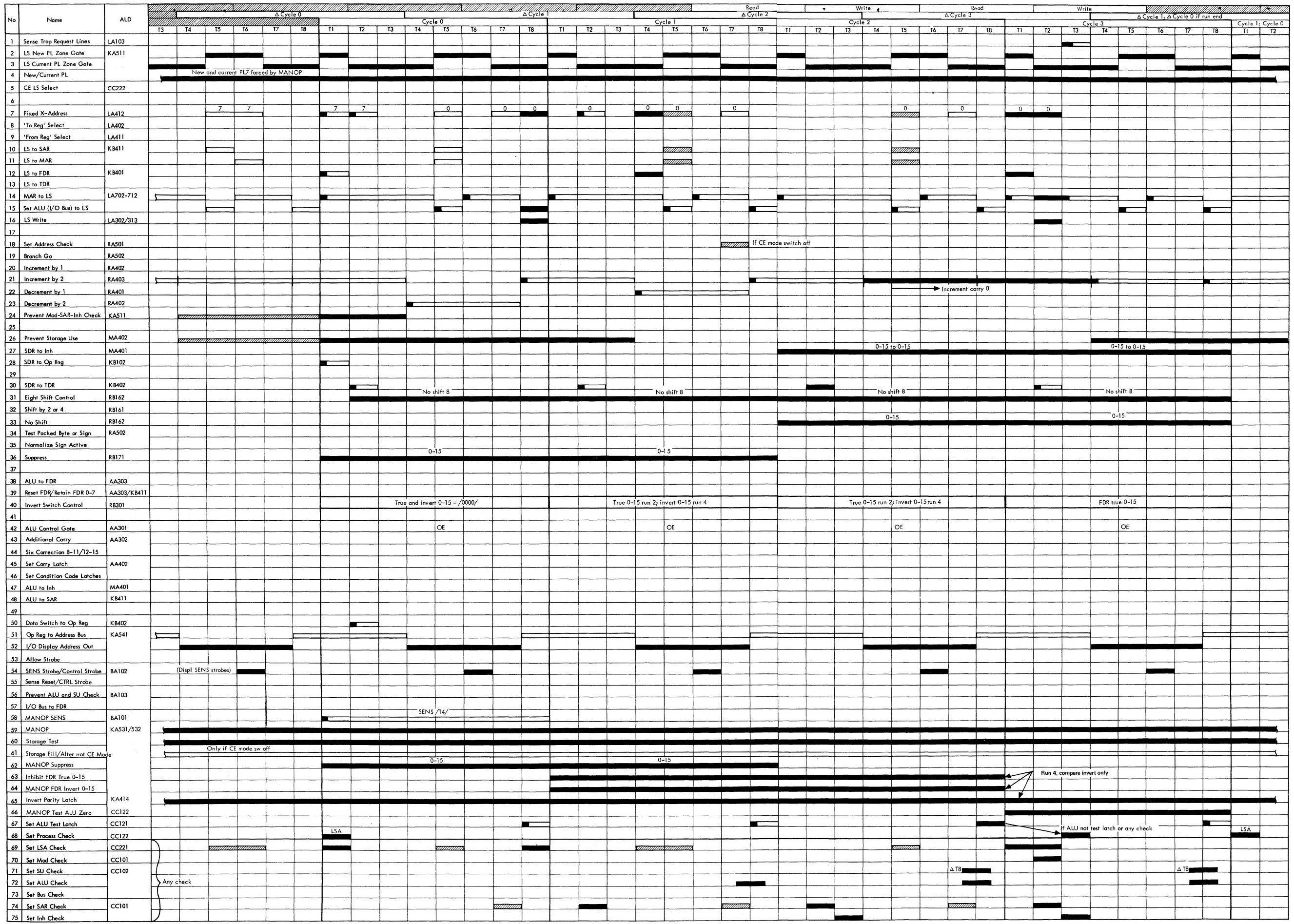
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:

Δ Cycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.



Function signals: Δ Cycle (diagonal hatching), Cycle (solid black), Δ Cycle (white), Cycle (white).

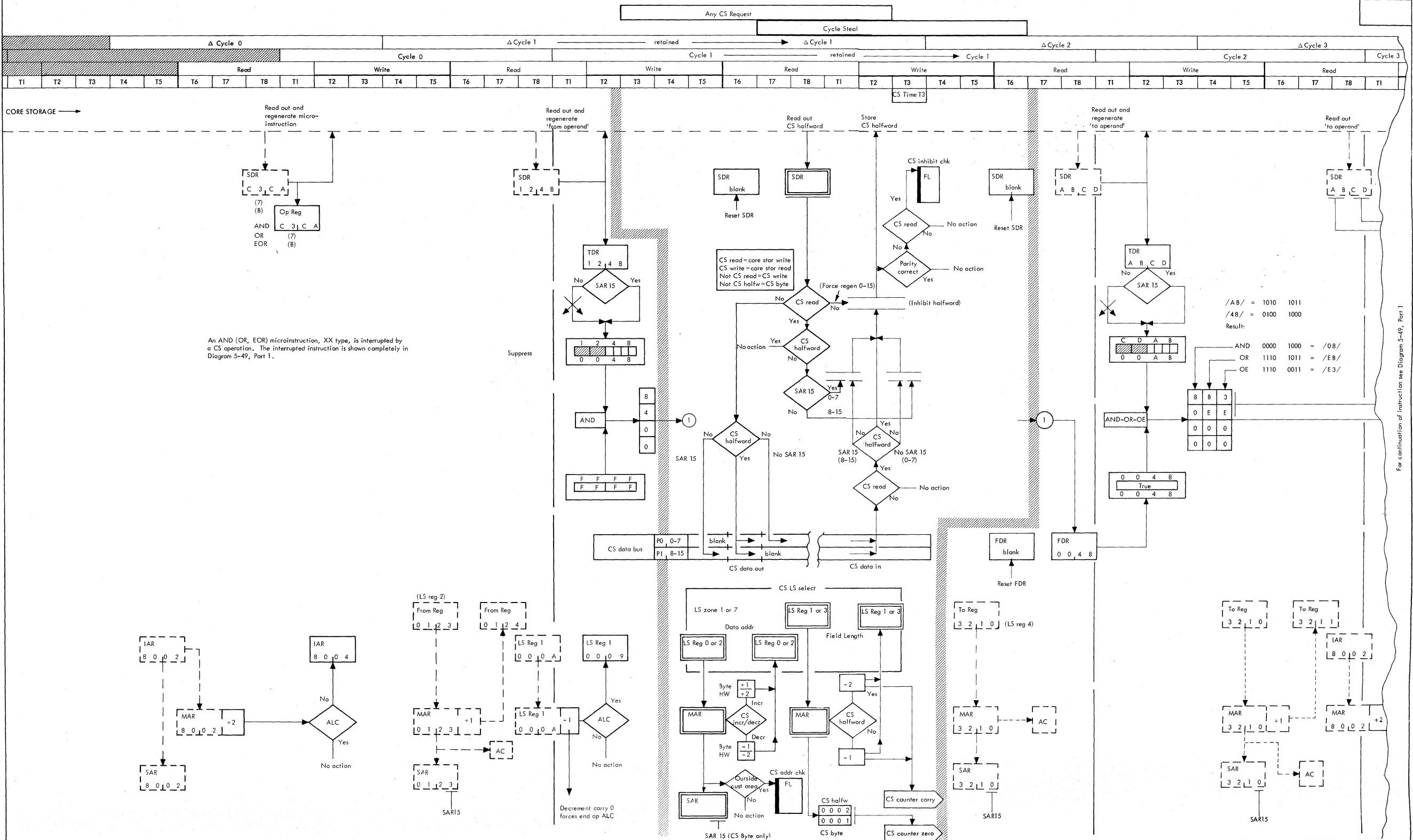
"Do not care" signals: Δ Cycle (white), Cycle (white).

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20. (Machines with serial no 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

Note: For "Do not care" functions refer to timing chart below.

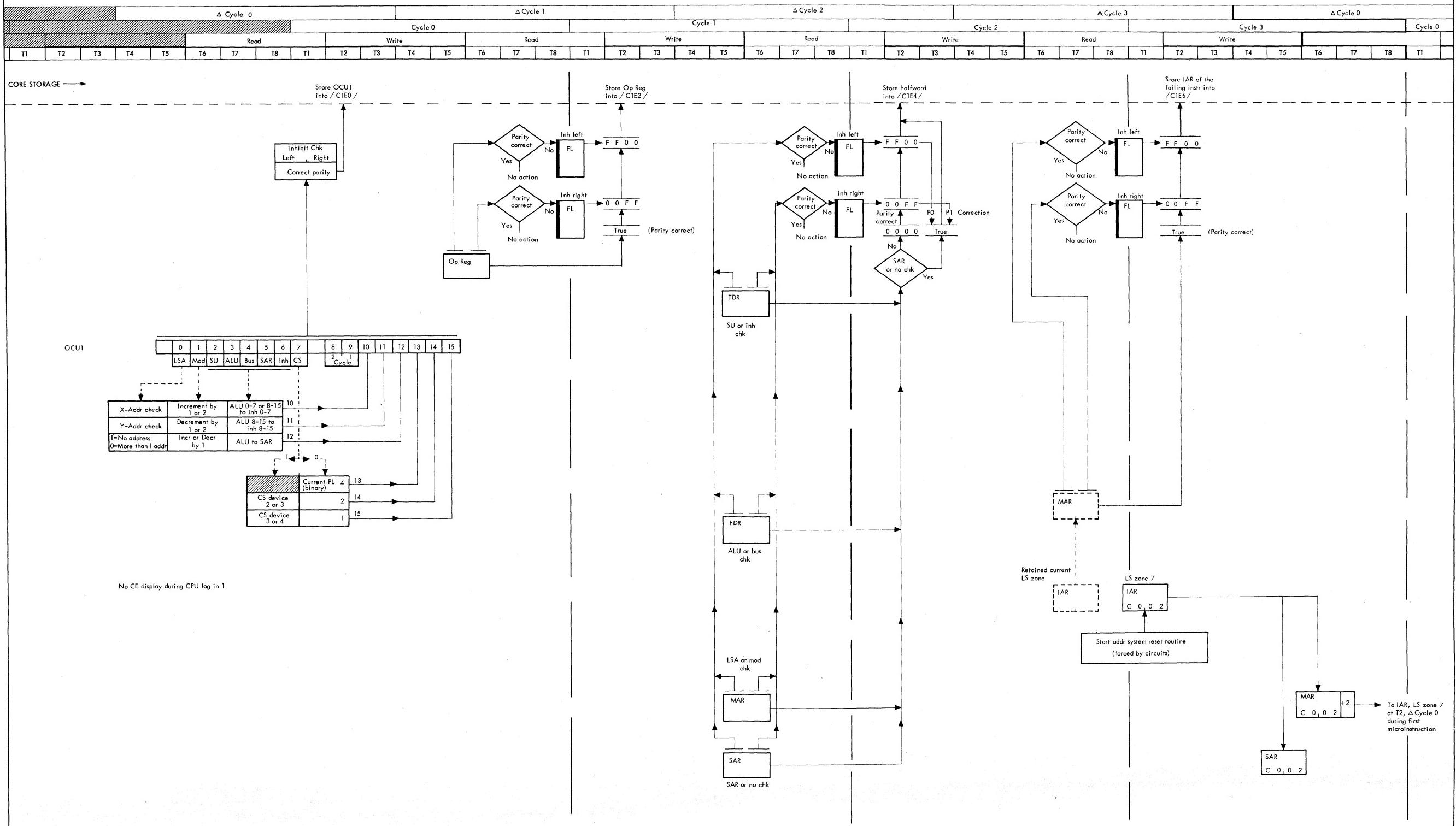
"Do not care" signals:
 Δ Cycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

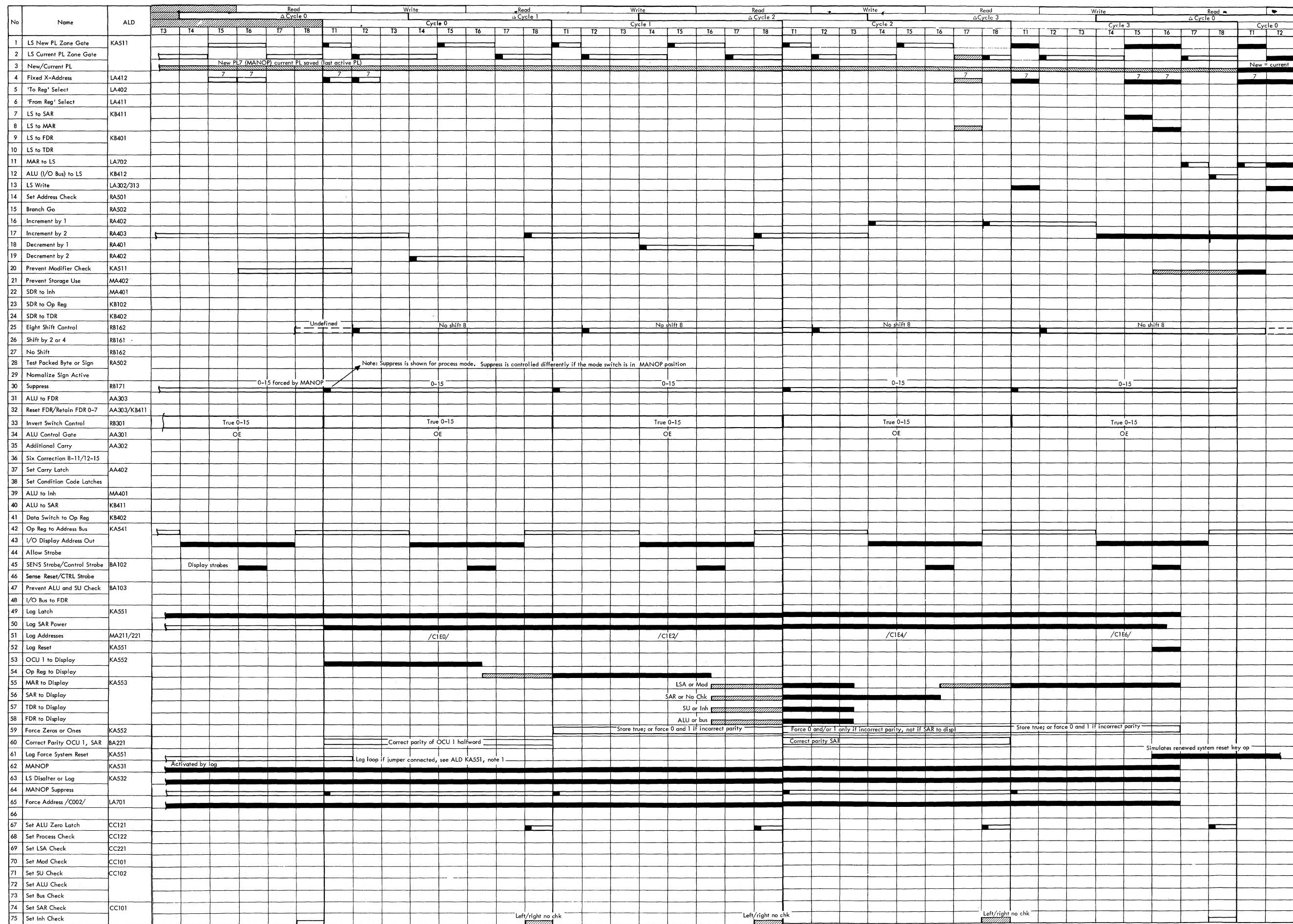
Mnemonic	
Format	
Type	
Cycle	



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
 ΔCycle []
 Cycle []



Function signals: △Cycle Cycle "Do not care" signals: △Cycle Cycle



Function signals: Δ Cycle [diagonal hatching] Cycle [solid black]

"Do not care" signals: Δ Cycle [white] Cycle [white]

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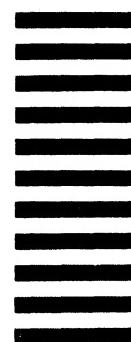
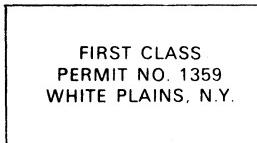
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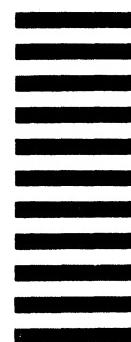
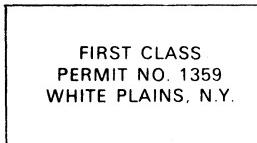
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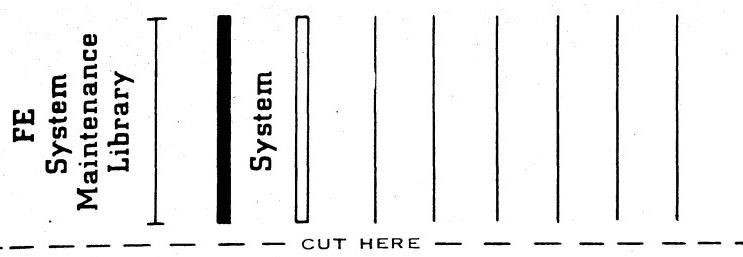
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